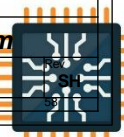


<Variant Name>

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Title **Power Block Diagram**

Size A3 Document Number **KARIA - DISCRETE**
Date: Friday, May 16, 2008 Sheet 53 of 53



Voltage Rails

o MEANS ON x MEANS OFF

power plane State	+BB LDO3 LDO5	+3VALW +5VALW	+1.8V +5V +0.9v	+5VS +3VS +1.8VS +1.5VS +VGA_CORE +CPU_CORE +VCCP	+3VM +1.05VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	O	O
S5 S4/Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader&l394	AD25	2	G,E

PCIE Devices

DEVICE	NUMBER	CHANNEL
UWB(no support)	1	1
WLAN	1	2
EXPRESS CARD	1	3
WWLAN	1	4
DOCKING	1	5
GIGA LAN	1	6

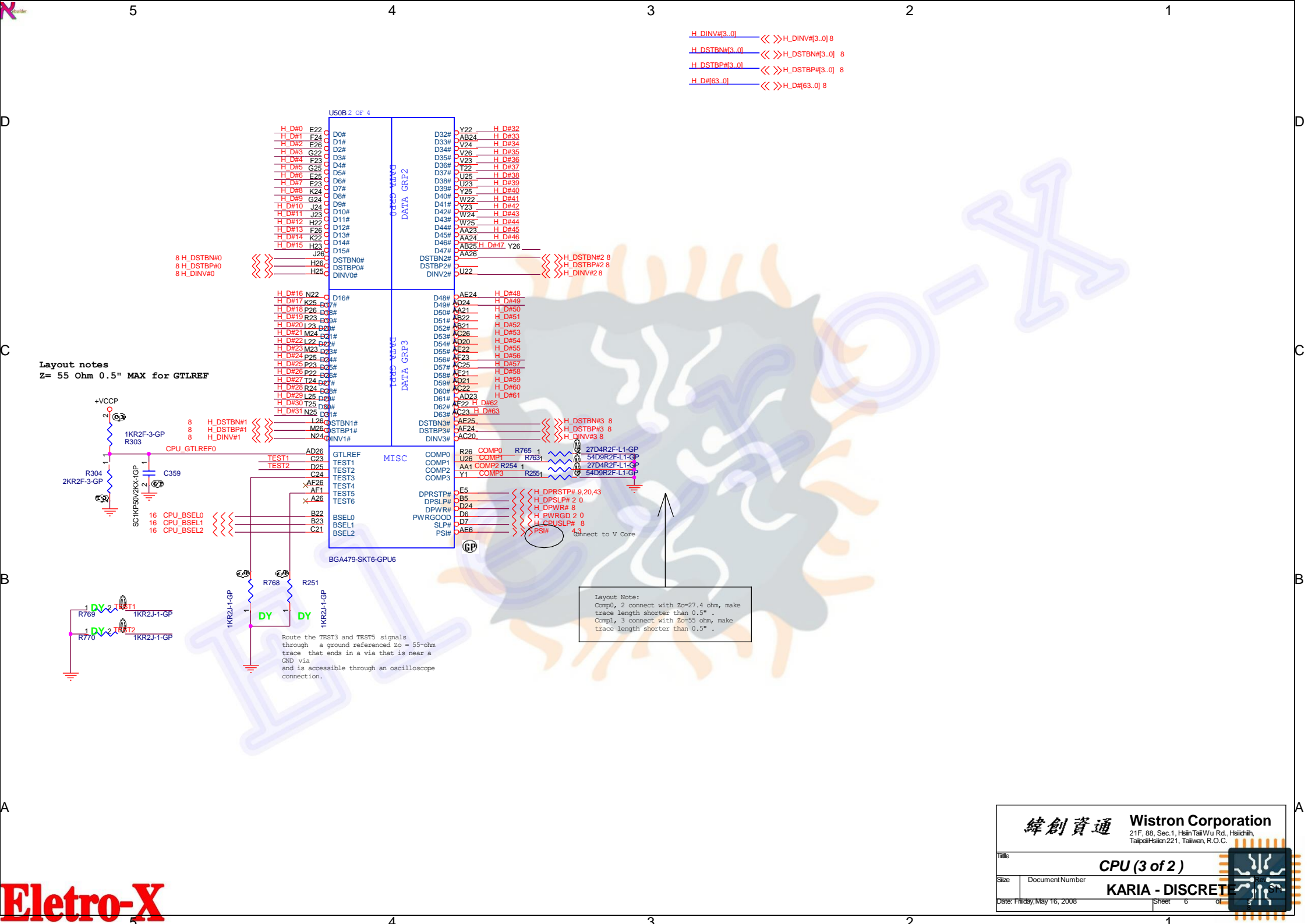
USB PORT	Device
0	USB1
1	Free
2	EX-P
3	WLAN
4	USB2
5	USB3
6	BLUETOOTH
7	WWAN
8	FignerPrint
9	Dock1
10	WEBCAM
11	DOCK2

Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything
1U16V2ZY-2GP	Caps 1U ,Size 0402 Y5V
2D2U6D3V3MX	Caps 2.2U ,Size 0603 X5R

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	Floppy
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH9 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH9 Family) PCI Express Root Port -27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH9 Family) USB Universal Host Control
18	Intel 82801H (ICH9 Family) USB Universal Host Control Richo R5C835 Integrates FlashMedia Control Richo R5C835 Gemcore based SmartCard Control
19	Intel 82801H (ICH9 Family) PCI Express Root Port -27D6 Intel 82801H (ICH9 Family) USB Universal Host Control
20	Intel 82801H (ICH9 Family) USB Universal Host Control Intel 82801H (ICH9 Family) USB2 Enhanced Host Control
21	Intel 82801H (ICH9 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control
23	HP Mobile Data Protection Sensor

<Variant Name>

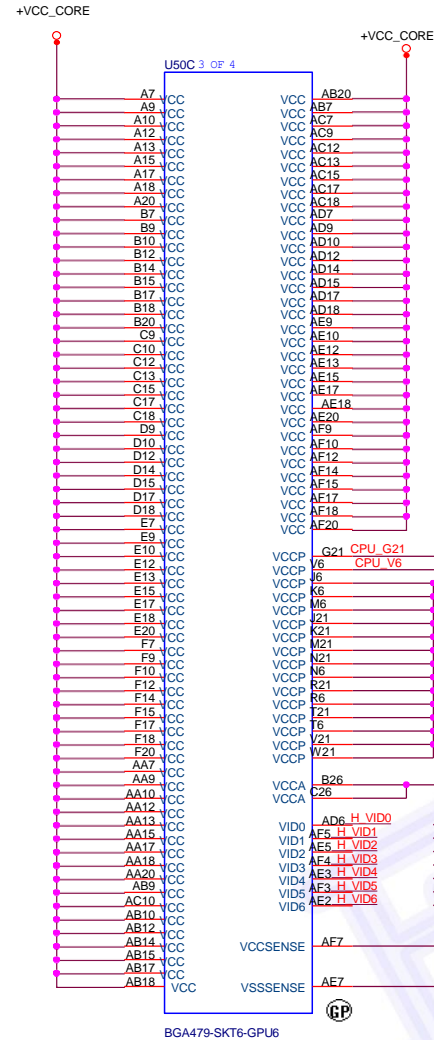
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Size A3		21F, 88, Sec.1, HsinTaiWu Rd., Hsichih, Taipei-Hsien 221, Taiwan, R.O.C.	
Date: Friday, May 16, 2008		Sheet 4 of 8	
Document Number		KARIA - DISCRETE	
Karia List		54	



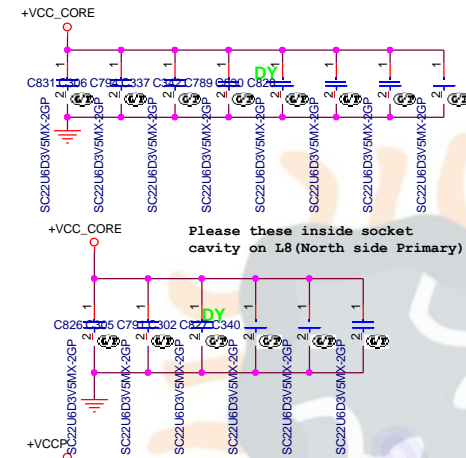
Layout notes
Z= 55 Ohm 0.5" MAX for GTLREF

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make
trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make
trace length shorter than 0.5" .

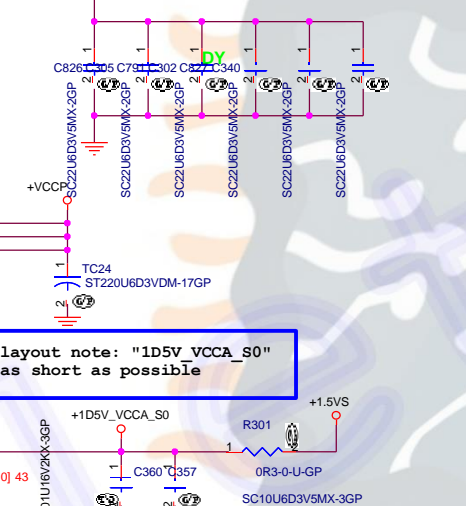
Please these inside socket cavity on L8(North side Secondary)



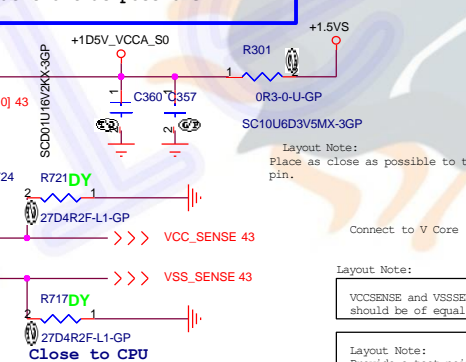
Please these inside socket cavity on L8(South side Secondary)



Please these inside socket cavity on L8(North side Primary)

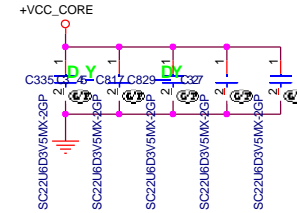


layout note: "1D5V VCCA_S0" as short as possible



Please these inside socket cavity on L8(North side Secondary)

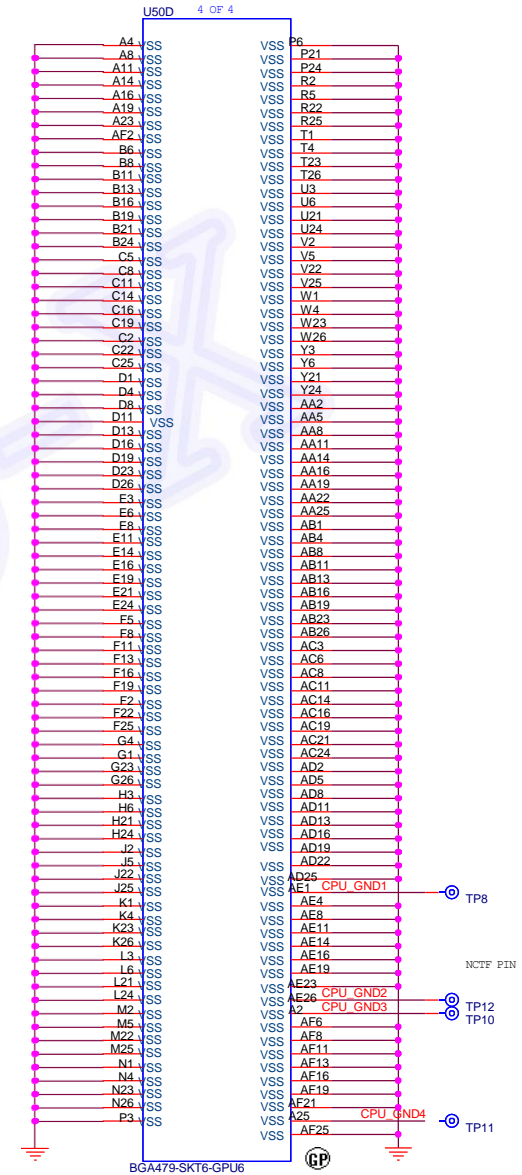
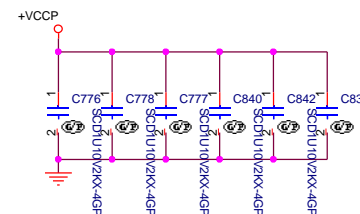
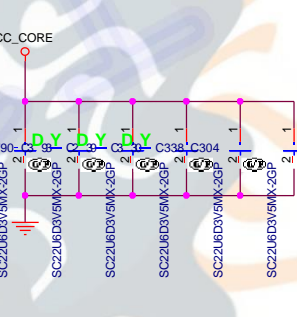
Please these outside socket cavity on L8(North side Secondary)



Please these outside socket cavity on L8(South side Secondary)



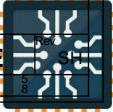
Please these inside socket cavity on L8(South side Primary)



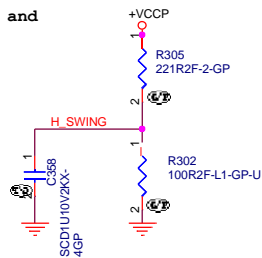
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CPU (3 of 3)

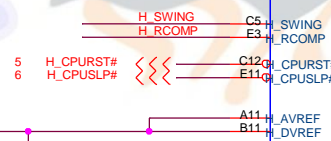
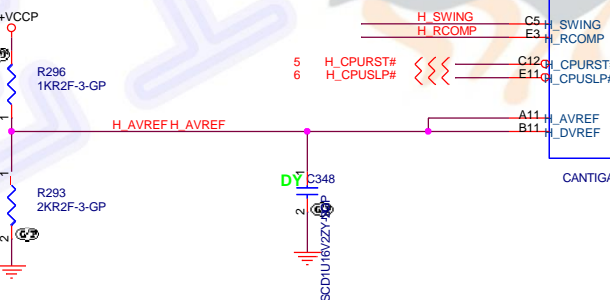
Size Document Number KARIA - DISCRETE
Date: Friday, May 16, 2008 Sheet 7 of 7



H_SWING Resistors and
Capacitors close MCH
500 mil (MAX)



Place them near to the chip (< 0.5")



CANTIGA-GM-GP-U-NF

1 OF 10

H_A#[35..3]

H_A#[35..3] << >> H_A#[35..3] 5

H_A# 5	C14	H_A# 3
H_A# 4	C15	H_A# 4
H_A# 5	F16	H_A# 5
H_A# 6	H13	H_A# 6
H_A# 7	C18	H_A# 7
H_A# 8	M16	H_A# 8
H_A# 9	J13	H_A# 9
H_A# 10	P16	H_A# 10
H_A# 11	R16	H_A# 11
H_A# 12	N17	H_A# 12
H_A# 13	M13	H_A# 13
H_A# 14	E17	H_A# 14
H_A# 15	F17	H_A# 15
H_A# 16	F17	H_A# 16
H_A# 17	G20	H_A# 17
H_A# 18	B19	H_A# 18
H_A# 19	J16	H_A# 19
H_A# 20	E20	H_A# 20
H_A# 21	H16	H_A# 21
H_A# 22	J20	H_A# 22
H_A# 23	L17	H_A# 23
H_A# 24	A17	H_A# 24
H_A# 25	B17	H_A# 25
H_A# 26	L16	H_A# 26
H_A# 27	C21	H_A# 27
H_A# 28	J17	H_A# 28
H_A# 29	H20	H_A# 29
H_A# 30	B18	H_A# 30
H_A# 31	K17	H_A# 31
H_A# 32	E20	H_A# 32
H_A# 33	G21	H_A# 33
H_A# 34	J21	H_A# 34
H_A# 35	Q21	H_A# 35

H_ADST#	H12	H_ADST# 5
H_ADSTB#_0	H16	H_ADSTB#0 5
H_ADSTB#_1	G17	H_ADSTB#1 5
H_BNR#	B9	H_BNR# 5
H_BPRI#	F1	H_BPRI# 5
H_BREQ#	G12	H_BREQ#0 5
H_DEFERR#	H_OBSY#	H_DEFERR# 5
H_OBSY#	F10	H_OBSY# 5
HPLL_CLK	AH7	CLK_MCH_BCLK16
HPLL_CLK#	AH6	CLK_MCH_BCLK#16
H_DPWR#	H	H_DPWR# 6
H_DRDY#	F9	H_DRDY# 5
H_HIT#	F12	H_HIT# 5
H_HITM#	F12	H_HITM# 5
H_LOCK#	H11	H_LOCK# 5
H_TRDY#	F9	H_TRDY# 5

Diagram illustrating the pin configuration for the STM32F103C8T6 microcontroller, showing connections for various pins and their corresponding functions.

Pin Connections:

- H_DINV#** (Pin J8) connects to **H_DINV#[3..0]**
- H_DINV#_1** (Pin L3) connects to **H_DINV#[3..0]**
- H_DINV#_2** (Pin Y13) connects to **H_DINV#[3..0]**
- H_DINV#_3** (Pin Y1) connects to **H_DINV#[3..0]**
- H_DSTBN#** (Pin L10) connects to **H_DSTBN#[3..0]**
- H_DSTBN#_1** (Pin M7) connects to **H_DSTBN#[3..0]**
- H_DSTBN#_2** (Pin A5) connects to **H_DSTBN#[3..0]**
- H_DSTBN#_3** (Pin AE6) connects to **H_DSTBN#[3..0]**
- H_DSTBP#** (Pin I9) connects to **H_DSTBP#[3..0]**
- H_DSTBP#_1** (Pin M8) connects to **H_DSTBP#[3..0]**
- H_DSTBP#_2** (Pin AA6) connects to **H_DSTBP#[3..0]**
- H_DSTBP#_3** (Pin AC5) connects to **H_DSTBP#[3..0]**
- H_REQ#** (Pin B15) connects to **H_REQ#[4..0]**
- H_REQ#_1** (Pin K13) connects to **H_REQ#[4..0]**
- H_REQ#_2** (Pin F13) connects to **H_REQ#[4..0]**
- H_REQ#_3** (Pin H) connects to **H_REQ#[4..0]**
- H_REQ#_4** (Pin B14) connects to **H_REQ#[4..0]**
- H_RS#** (Pin B6) connects to **H_RS#[2..0]**
- H_RS#_1** (Pin F12) connects to **H_RS#[2..0]**
- H_RS#_2** (Pin C8) connects to **H_RS#[2..0]**

<Variant Name>

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Title

Size

Document Number

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Cantiga (1 of 6)

KARIA - DISCRE

Sheet 8

Eletro-X

Strap Pin Table 5

CFG[2:0] FSB Freq select	000 = FSB 1067MHz 010 = FSB 800MHz	011 = FSB 667MHz Others = Reserved
CFG4;3; 8; 11; 14; 15; 17; 18	Reserved	
CFG5 (DMI select)	Low = DMI x2 High = DMI x4 *	
CFG6 (ITPM Host Interface)	High = The ITPM Host Interface is disabled * Low = The ITPM Host Interface is enabled	
CFG7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS Cipher suite with confidentiality	
CFG9 (PCIe GraphicsLane)	Low = Reverse Lanes, 15->0, 14->1 etc. High = Normal operation:Lane Numbered in Order *	
CFG10 (PCIe Loopbackenable)	Low = Enabled High = Disabled *	
CFG12(ALLZ)	Low = ALLZ mode Enabled High = Disabled *	
CFG13(XOR)	Low = XOR mode Enabled High = Disabled *	
CFG16 (FSB DynamicODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled *	
CFG19 (DMI Lane Reversal)	Low = Noraml operation: Lane Numbered in Order * High = Reverse Lanes DMI x 4 mode[MCH->ICH]: (0->3, 2->1, 1->2 and 0->3) DMI x 2 mode[MCH->ICH]: (3->0, 2->1)	
CFG20 (Digital Display Port (SDVO/DP /HDMI) Concurrent with PCIe)	Low = Only Digital Display Port (SDVO/HDMI) or PCIe is operational * High = Digital Display Port (SDVO/DP/HDMI) and PCIe are operating simultaneously via the PEG port	
SDVO_CTRLDATA (SDVO Present)	Low = No SDVO Card Present * High = SDVO Card Present	
L_DDC_DATA (Local Flat Panel (LFP) Present)	Low = LFP Disabled * High = LFP Card Present; PCIe disabled	
DDPC_CTRLDATA (Digital Display Present)	Low = DisplayPort Disabled * High = DisplayPort Device Present	

FSB setting

5.16 MCH_CLKSEL0
5.16 MCH_CLKSEL1
5.16 MCH_CLKSEL2

CFG_0 ~ CFG_20

CFG 5, 7, 9, 10, 12, 13, 16, 19, 20
Teenah = 4.02K
Cantiga = 2.2K

Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time

ME_JTAG_TCK R843 1
ME_JTAG_TDI R839 1
ME_JTAG_TDO T839 1
ME_JTAG_TMS R844 1

Cantiga-GM-GP-U-NF


Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.

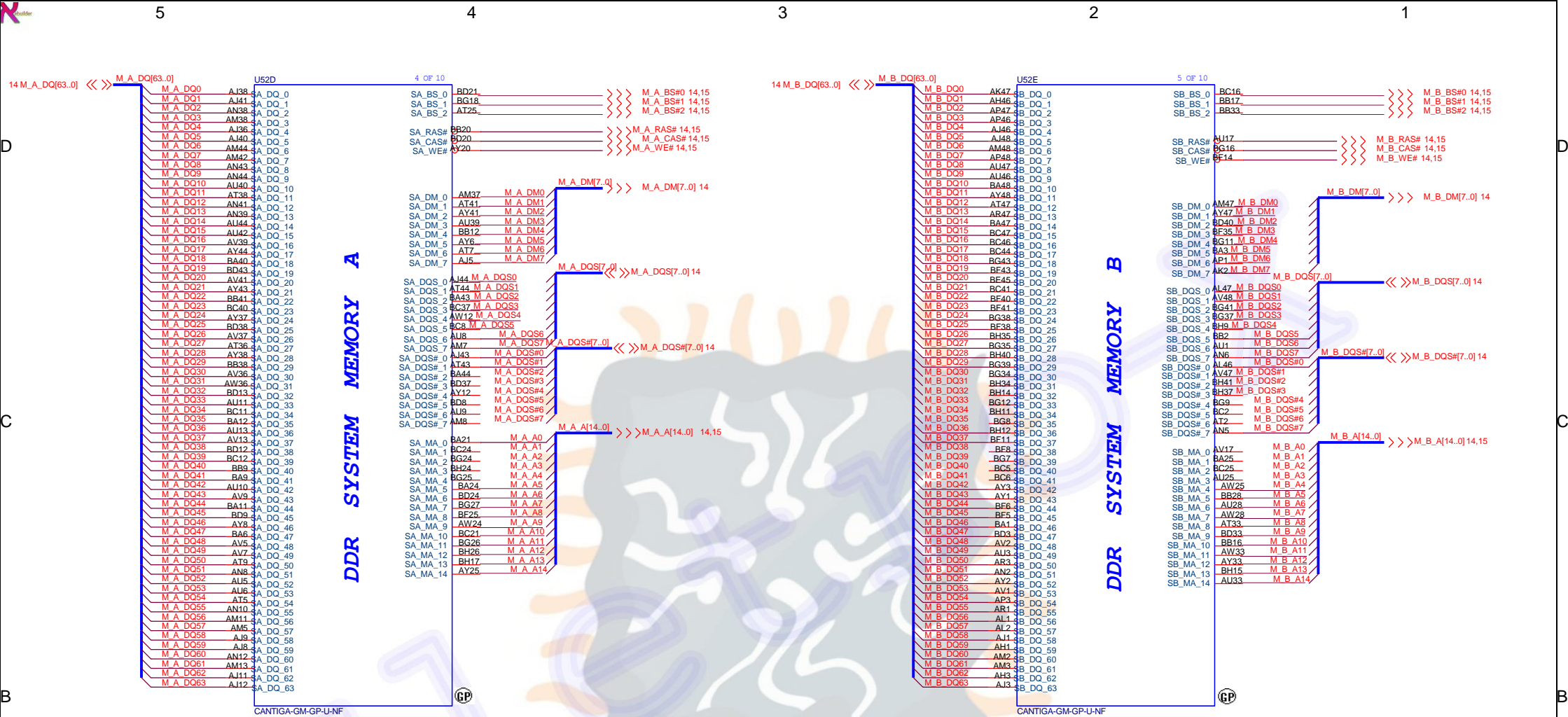
49.9 OHM FN:64.49R9S.6DL

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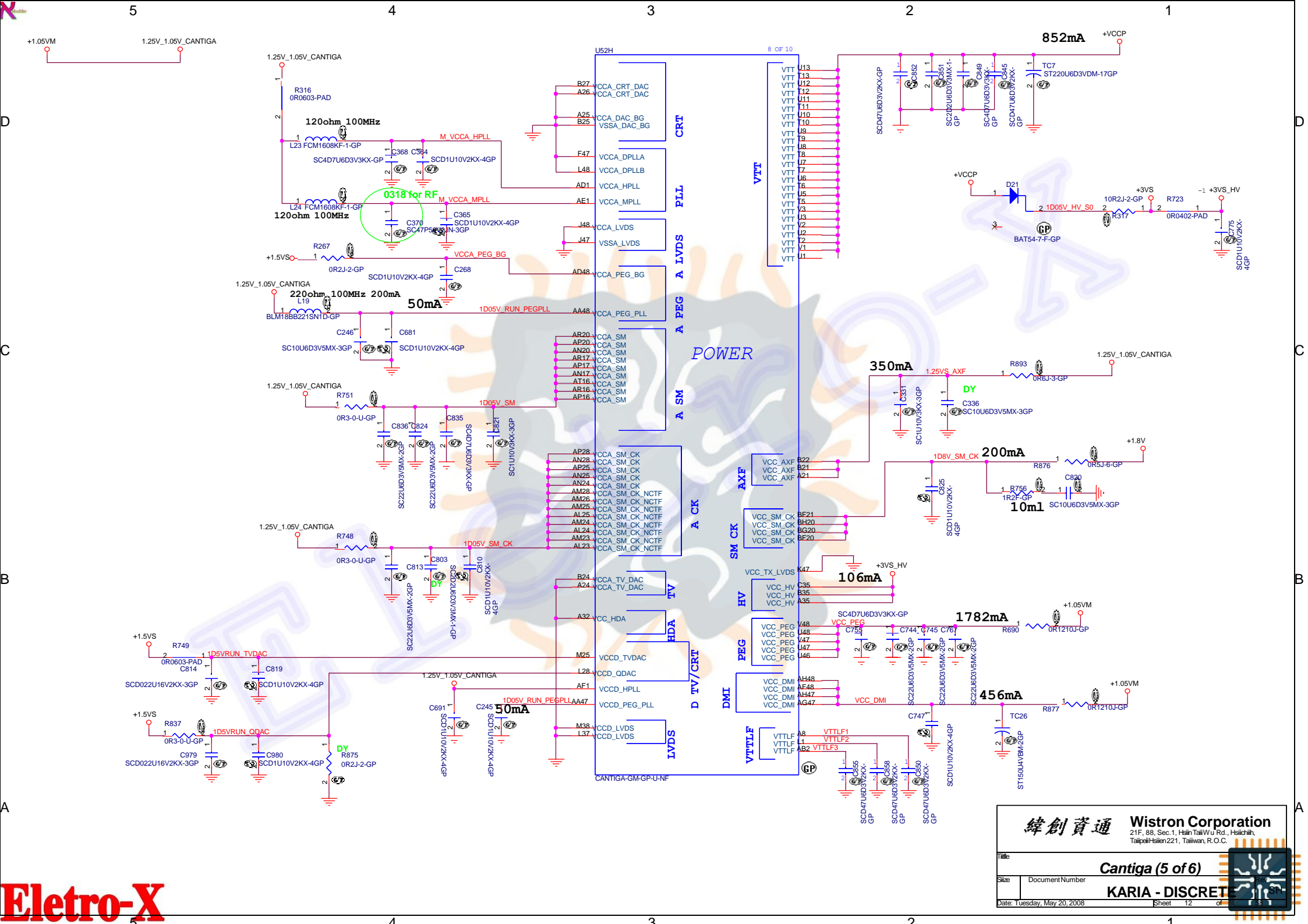
KARIA - DISCRETE

Date: Monday, May 19, 2008 Sheet 9 of 58

		Wistron Corporation 21F, 8th Sec. 1, Hsin TaiWu Rd., Hsichuan, Taipei/Hsien 221, Taiwan, R.O.C.	
Title			
<i>Cantiga (2 of 6)</i>			
Size	Document Number		Rev
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Date: Monday, May 19, 2008	Sheet	9 of	58



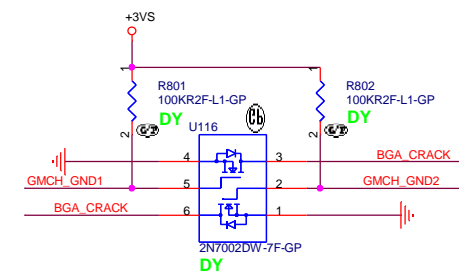
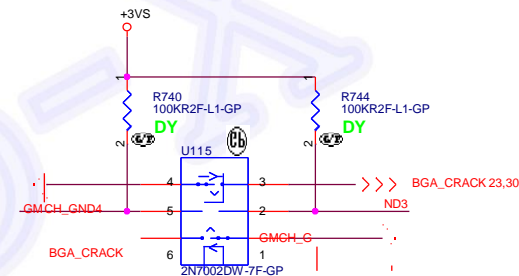
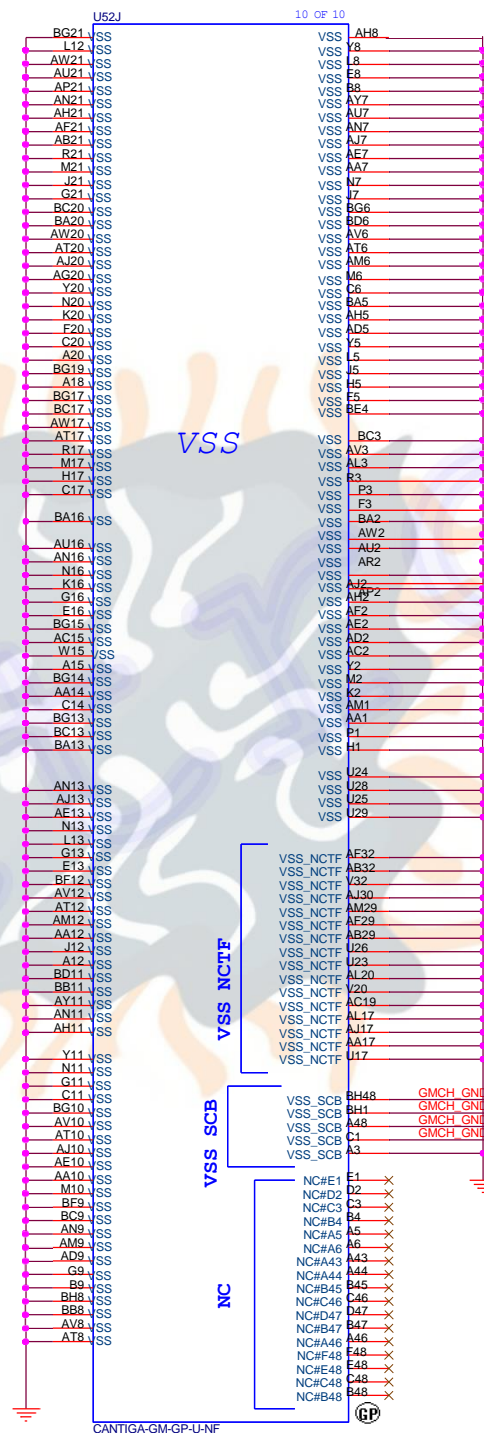
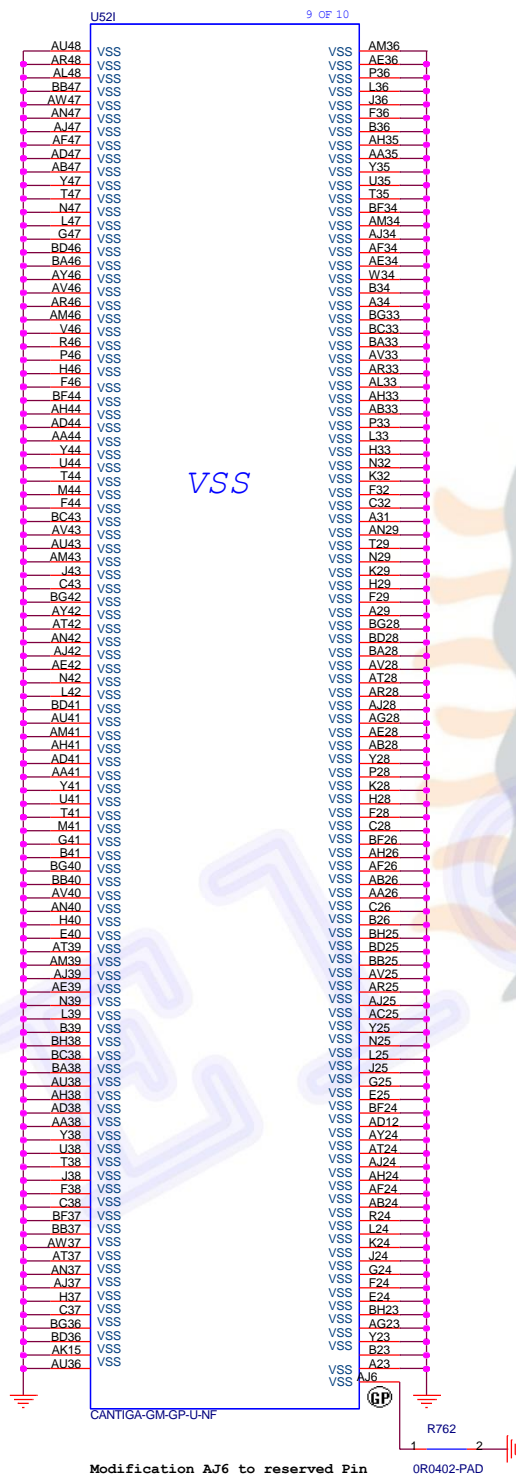




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Title		<i>Cantiga (5 of 6)</i>	
Size	Document Number	KARIA - DISCRET	Rev. SH
Date: Tuesday, May 20, 2008	Sheet	12	of 18

Eleto-X



NCTF PIN

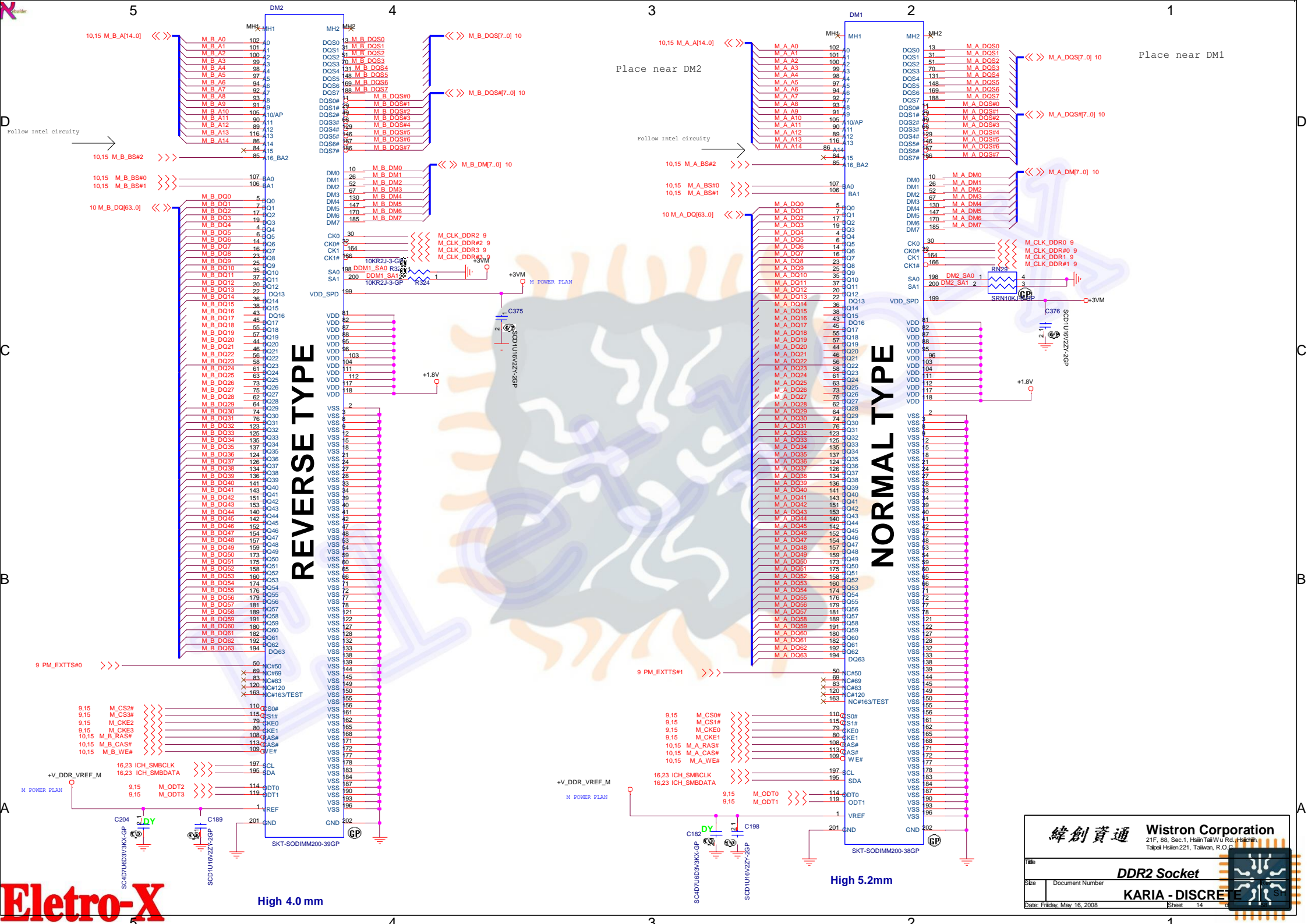
Pin	Signal	Function	TP
VSS_SCB	BH48	GMCH_GND1	TP6
VSS_SCB	BH1	GMCH_GND2	TP14
VSS_SCB	A48	GMCH_GND3	TP5
VSS_SCB	C1	GMCH_GND4	TP13
VSS_SCB	A3		

VSS SCB

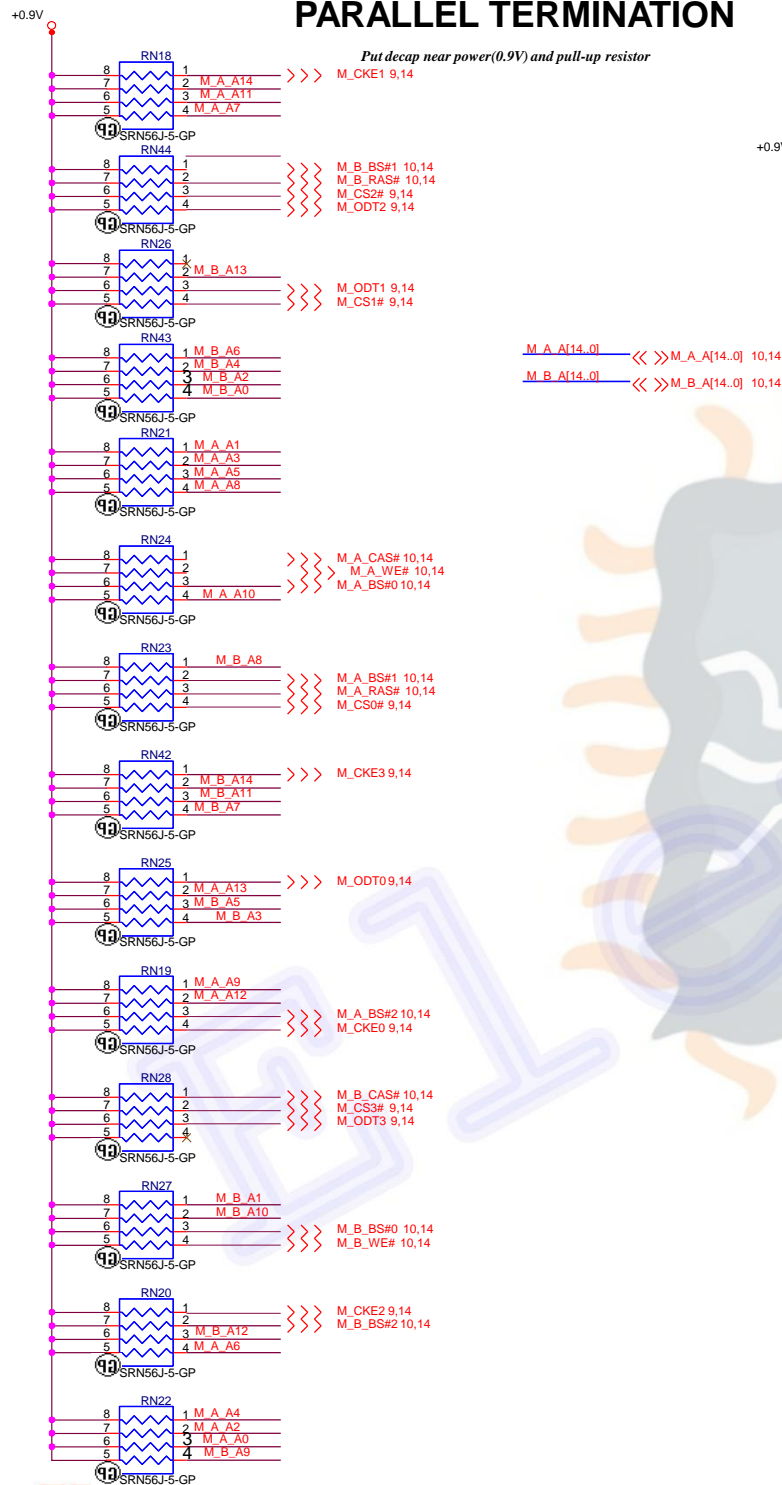
VSS NCTF

VSS

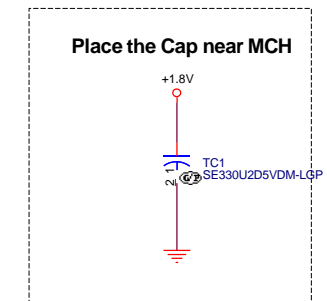
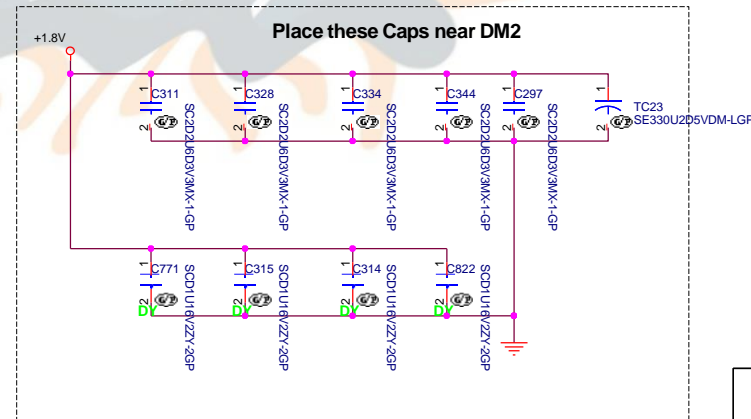
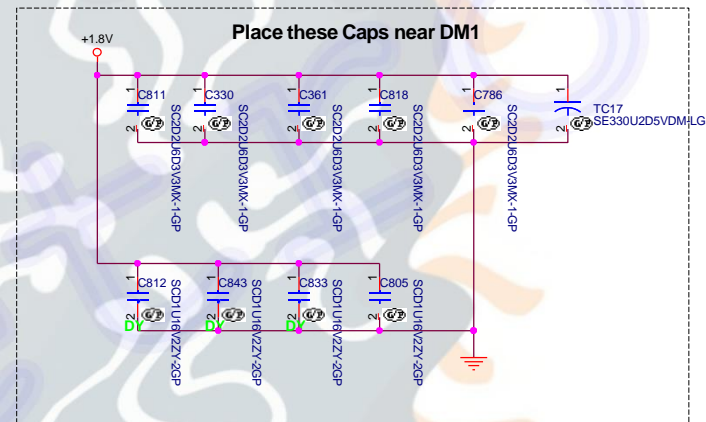
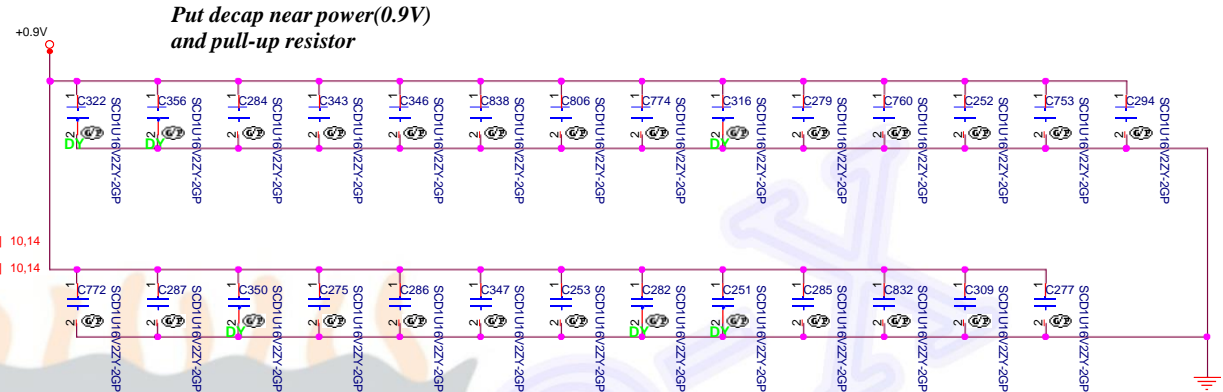
VSS



PARALLEL TERMINATION

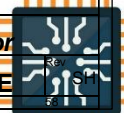


Decoupling Capacitor

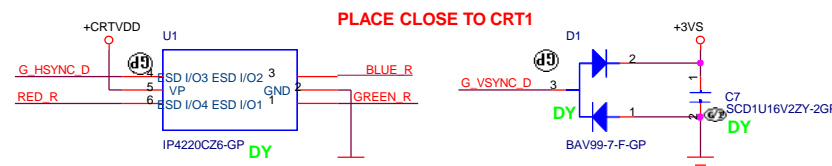
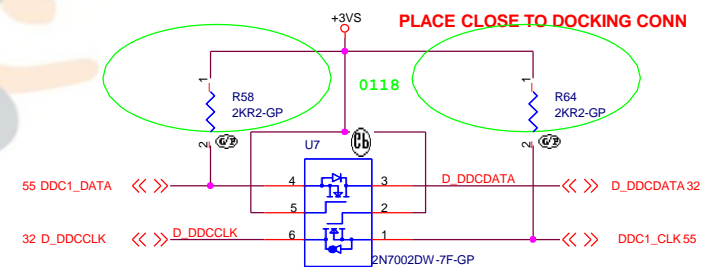


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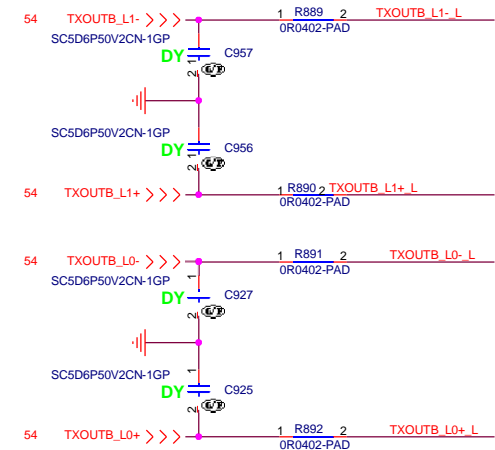
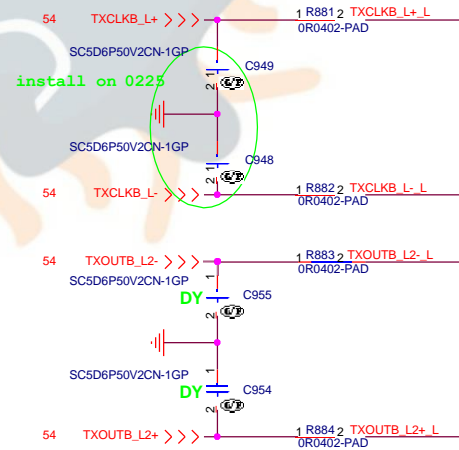
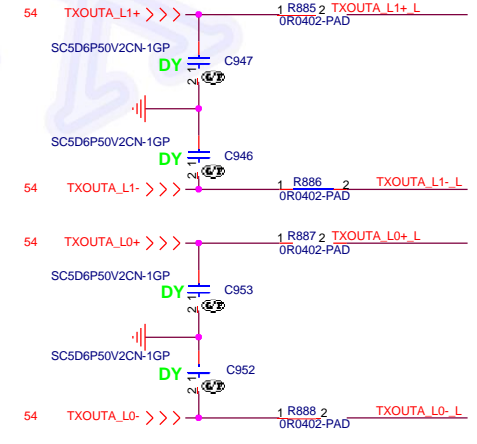
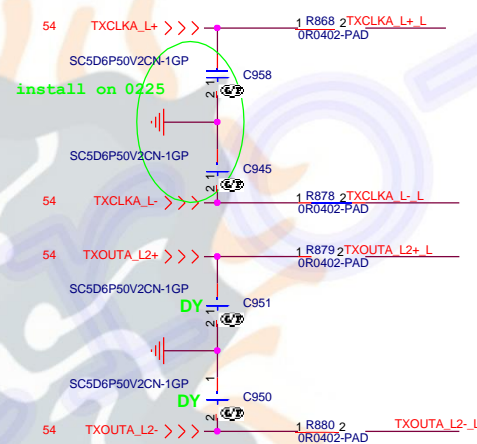
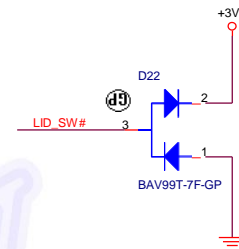
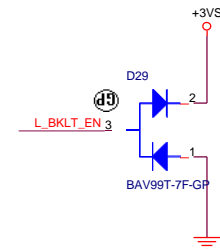
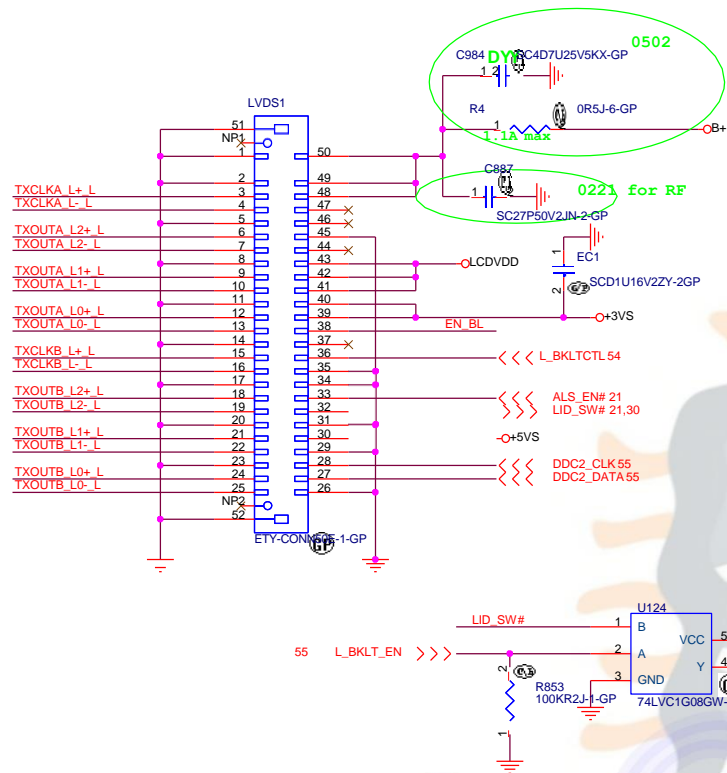
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Size: Document Number
Date: Friday, May 16, 2008
Sheet 15 of



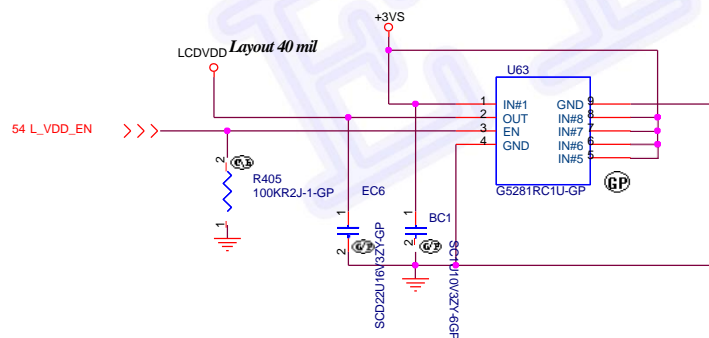
Eleto-X

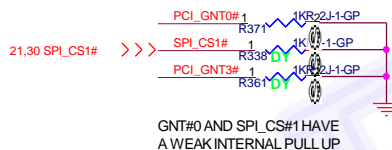
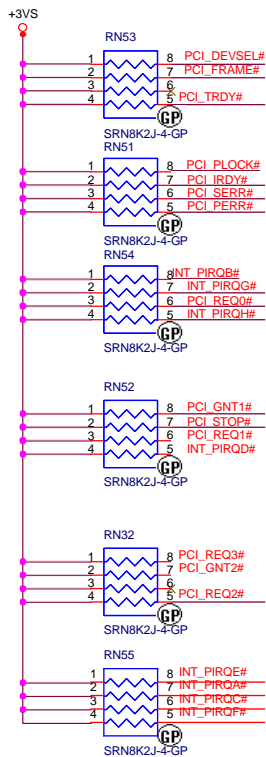


LVDS CONN

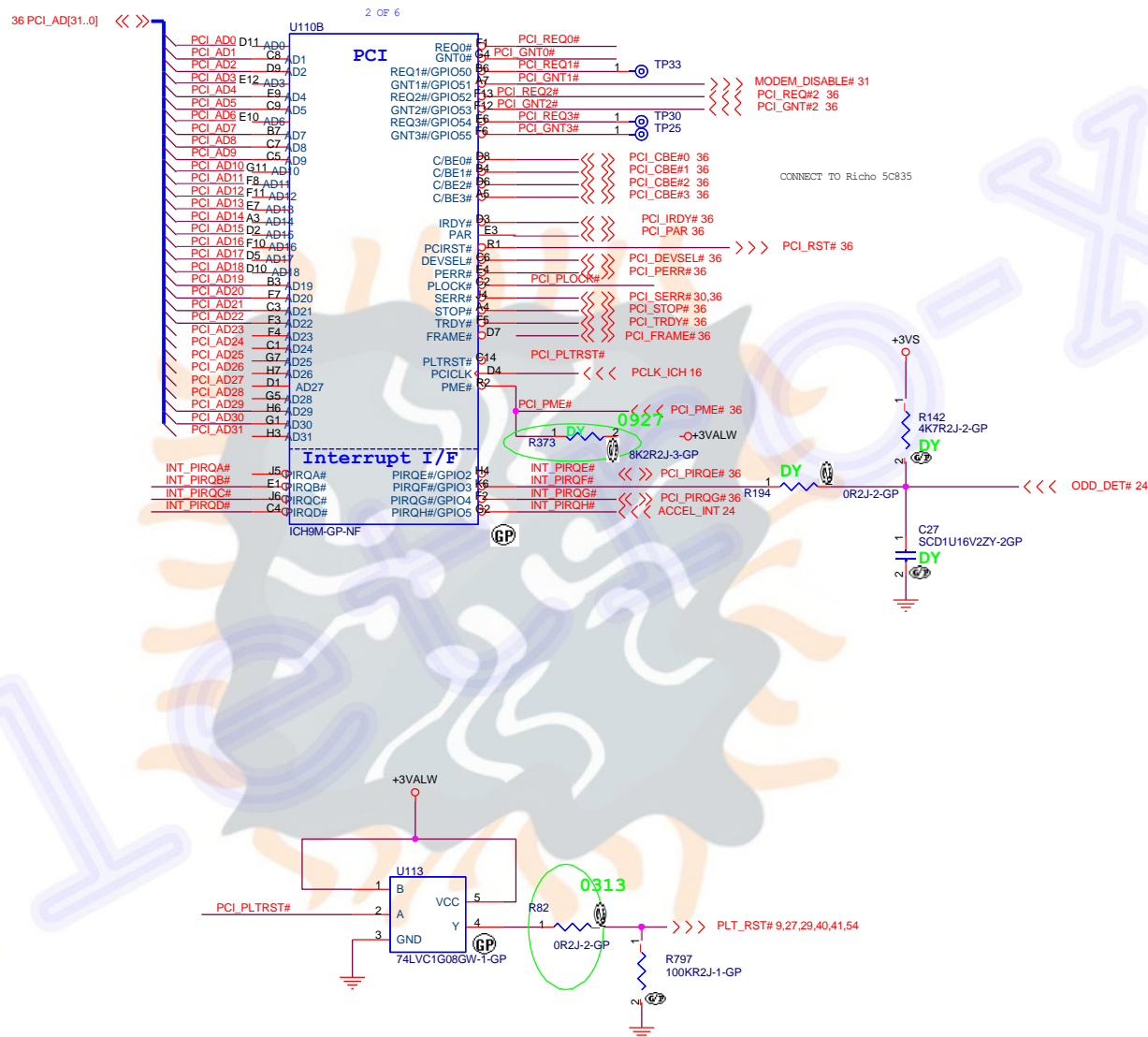


LCD POWER CIRCUIT





BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LFC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	



<Variant Name>

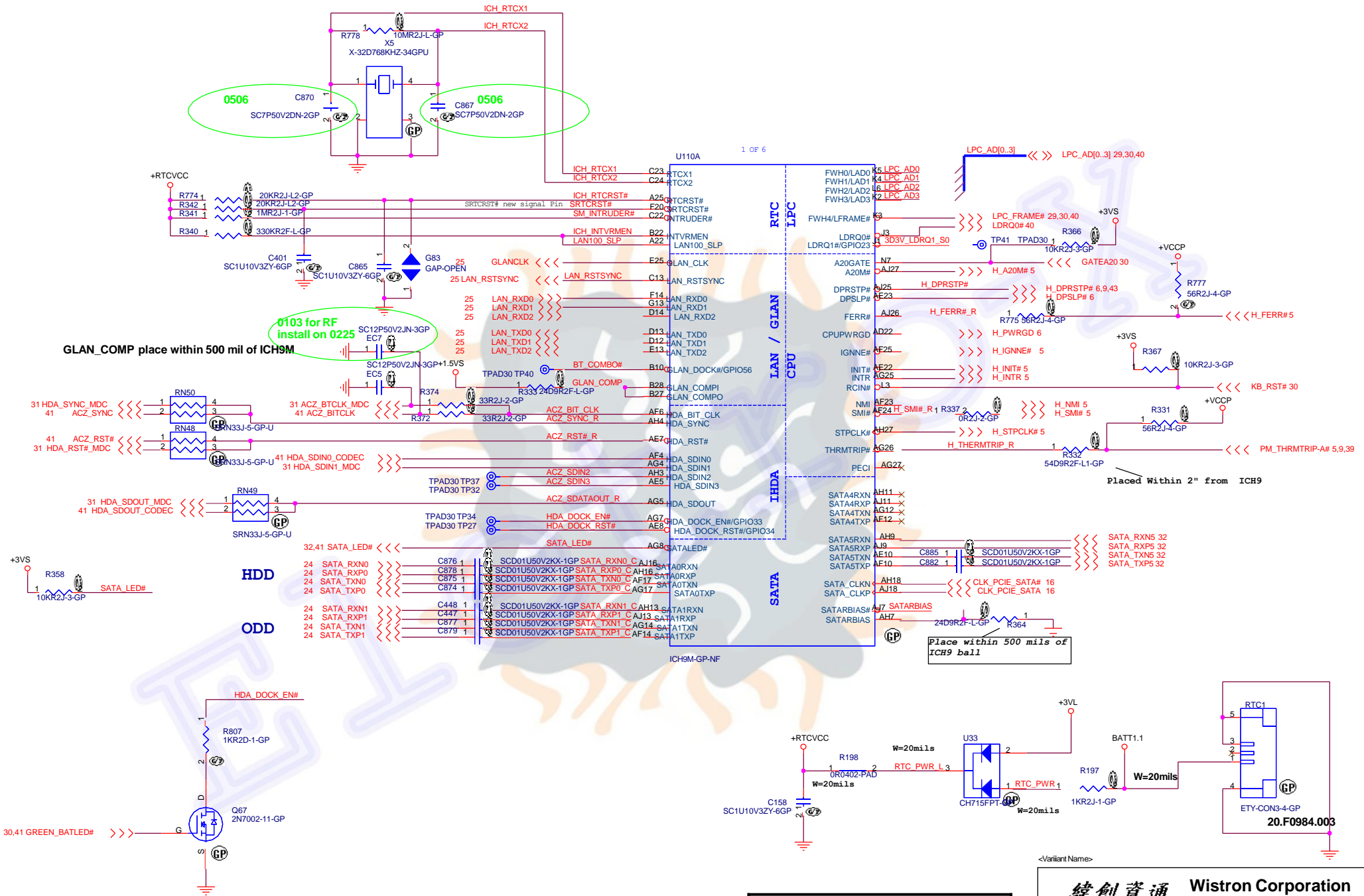
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Title: **ICH9-M (1 of 5)**

Size: Document Number: **KARIA - DISCRETE**

Date: Monday, May 19, 2008

Sheet 19 of



Integrated VccSus1_05,VccSus1_5,VccCl1_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCl1_05		
LAN100_SLP	High=Enable	Low=Disable

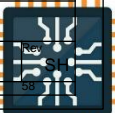
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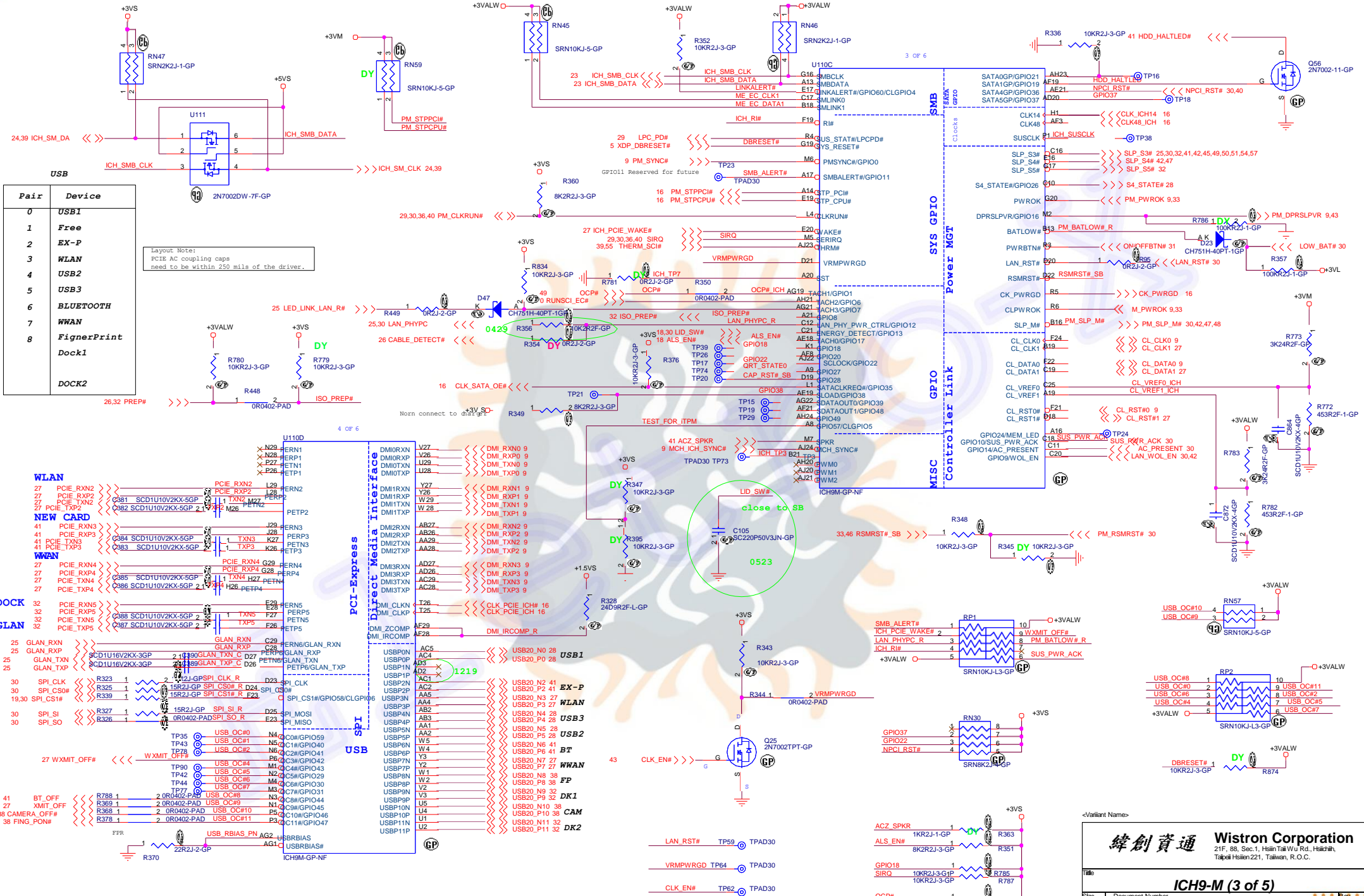
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Taipei-Hsien 221, Taiwan, R.O.C.

Title: **ICH9-M (2 of 5)**

Size: DocumentNumber: **KARIA - DISCRETE**

Date: Monday, May 19, 2008 Sheet 20 of





Pair	Device
0	USB1
1	Free
2	EX-P
3	WLAN
4	USB2
5	USB3
6	BLUETOOTH
7	WWAN
8	FignerPrint
	Dock1
	DOCK2

Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.

Pair	Device
0	USB1
1	Free
2	EX-P
3	WLAN
4	USB2
5	USB3
6	BLUETOOTH
7	WWAN
8	FignerPrint
	Dock1
	DOCK2

Pair	Device
0	USB1
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Pair	Device
0	USB1
1	Free
2	EX-P
3	WLAN
4	USB2
5	USB3
6	BLUETOOTH
7	WWAN
8	FignerPrint
	Dock1
	DOCK2

緯創資通

Wistron Corporation

21F, 88, Sec.1, HsinTai Wu Rd., Hsichih,
Taippei Hsien221, Taiwan, R.O.C.

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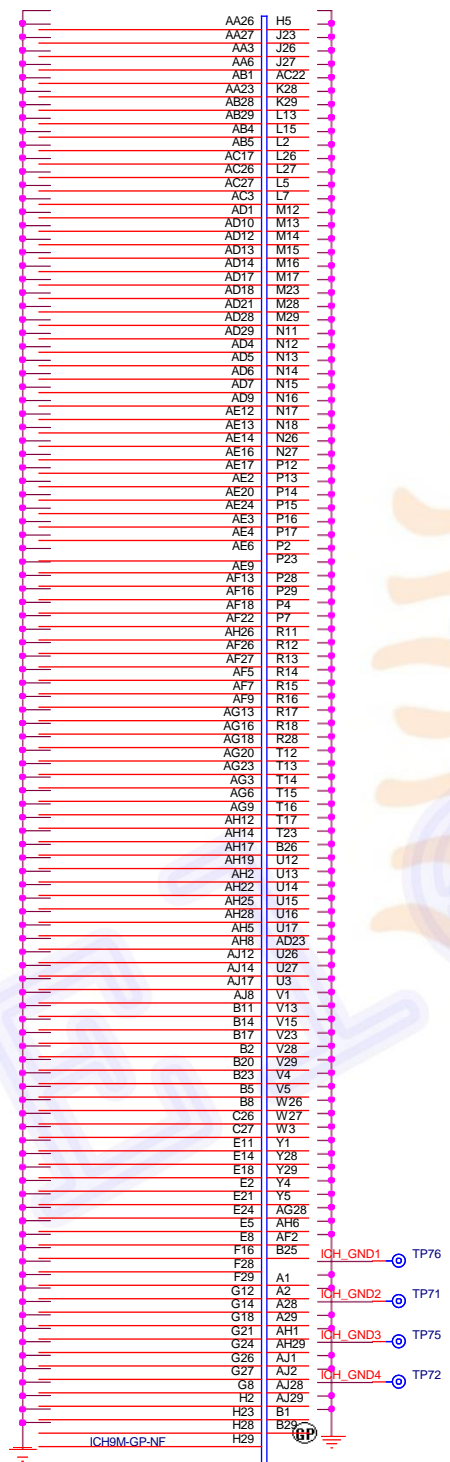
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Size Document Number

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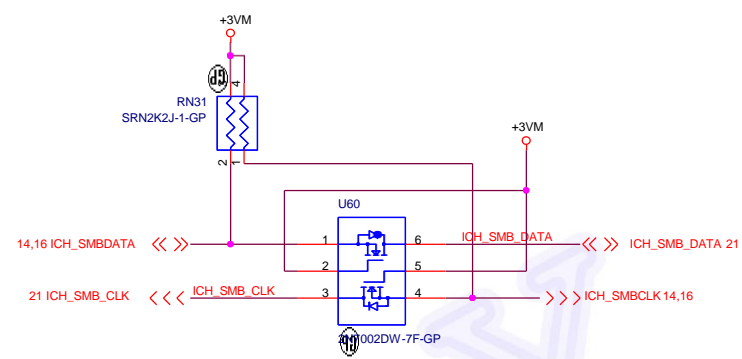
Date: Friday, May 23, 2008

Sheet 21

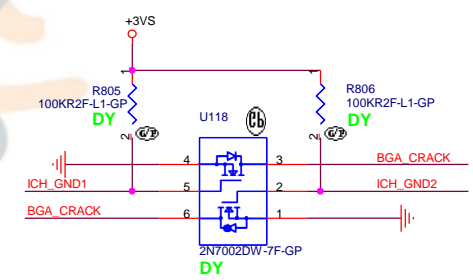
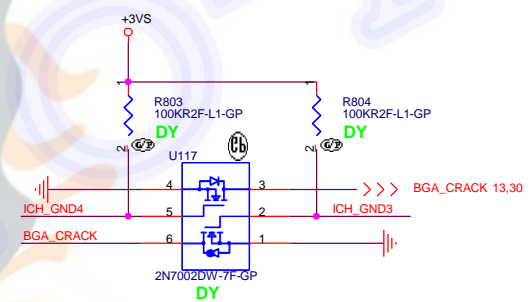


NCTF PIN

Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance



SMBUS



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File:

ICH9-M (5 of 5)

Size:

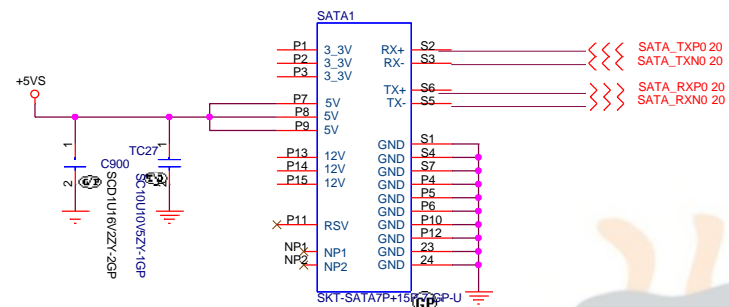
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Date: Friday, May 16, 2008

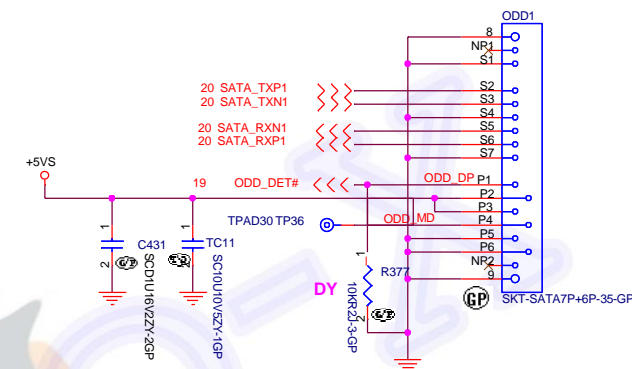
Sheet 23 of 23

KARIA - DISCRETE

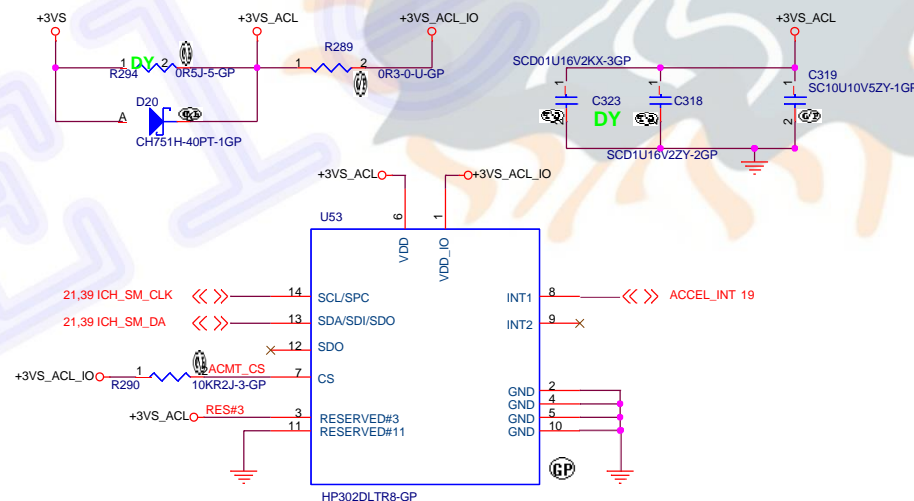
SATA HD Connector



ODD Connector



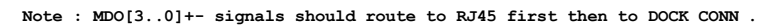
ACCELEROMETER



Must be placed in the center of the system

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, HsinTaiWu Rd., Hsichin, Taipei-Hsien221, Taiwan, R.O.C.	
Title	HDD/ODD/ACCELEROMETER
Size A3	Document Number
Date: Friday, May 16, 2008	KARIA - DISCRETE
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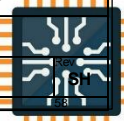


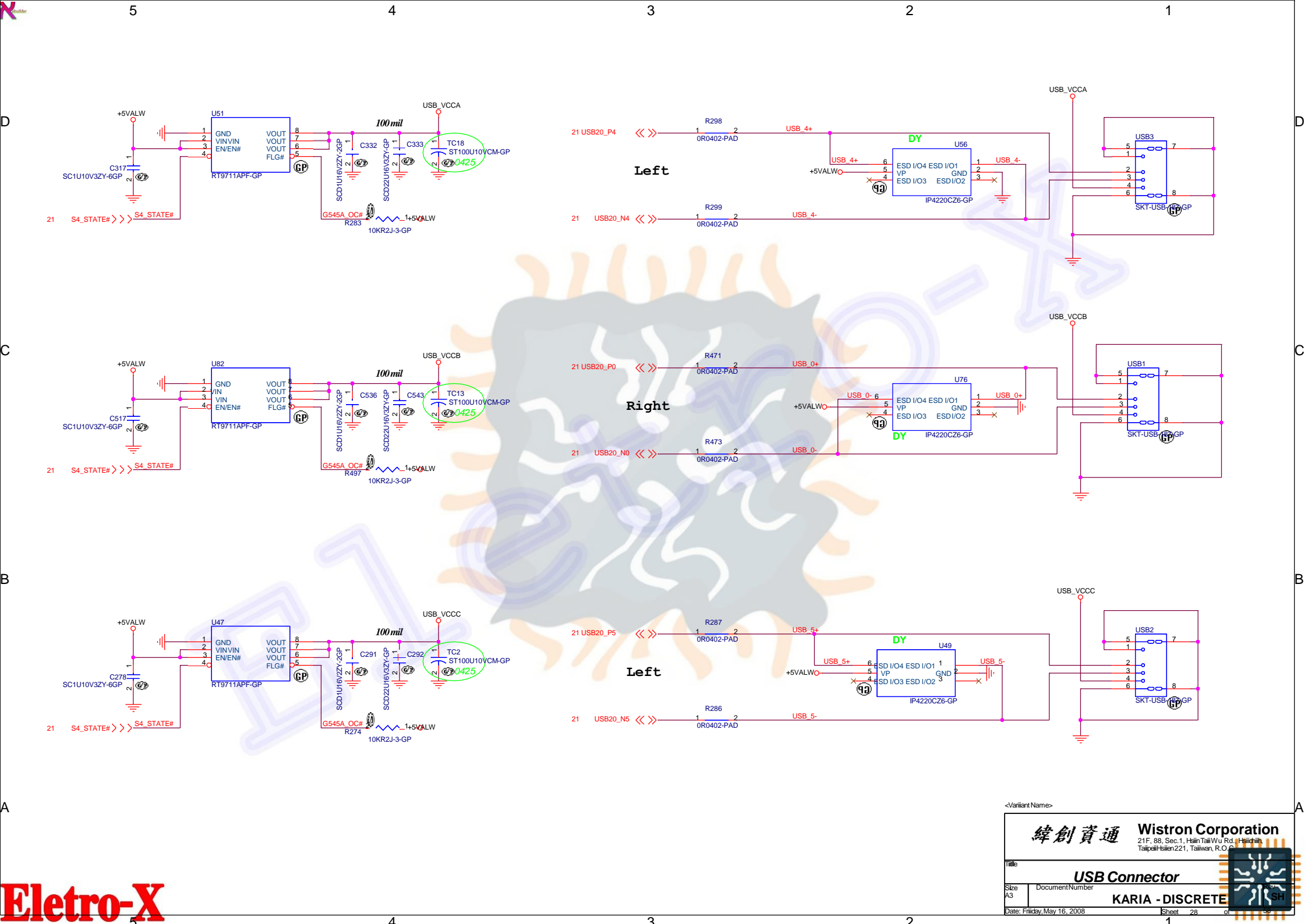
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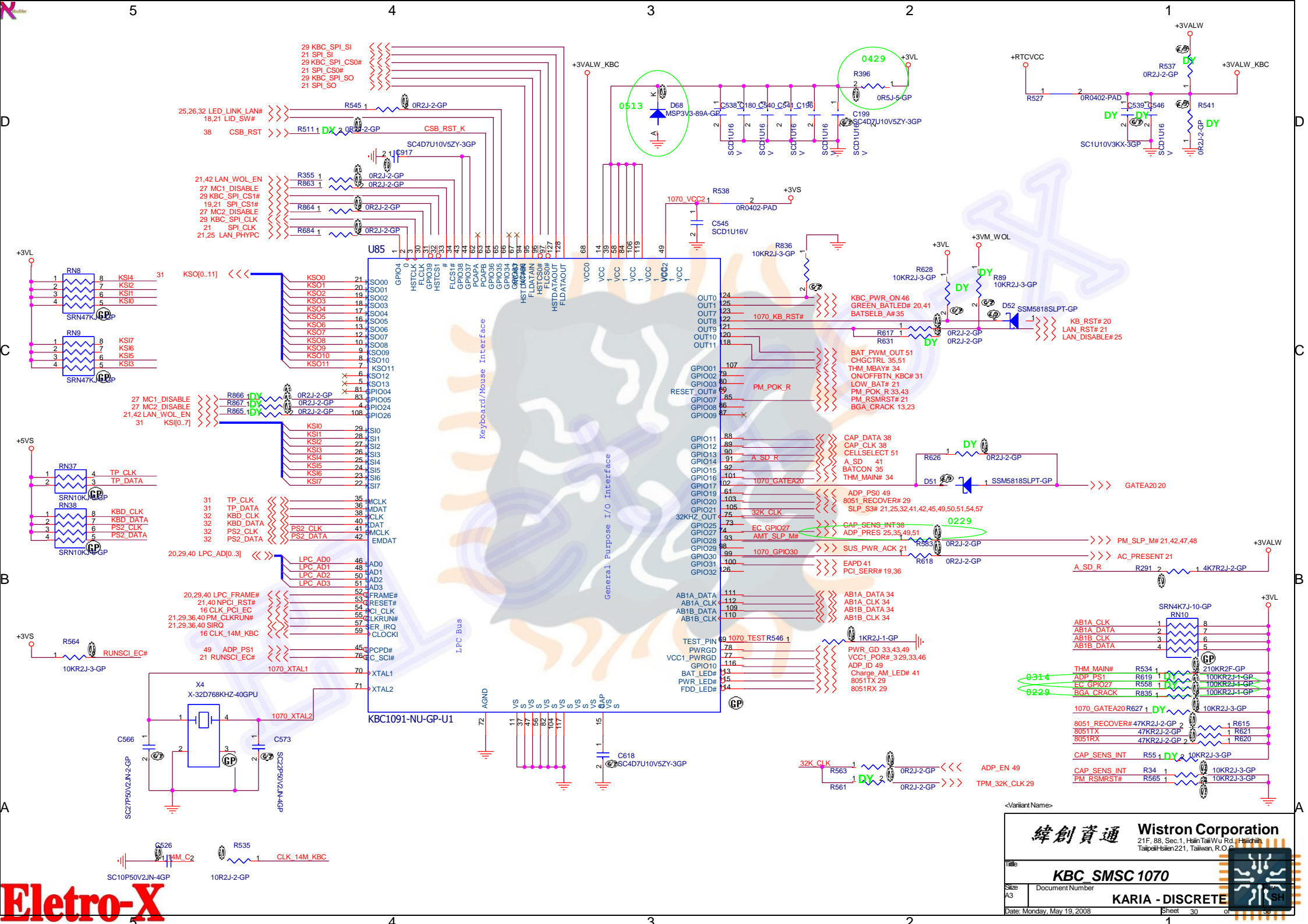


<Variant Name>

Title		Mini-Card connectors			
Size A3	DocumentNumber	KARIA - DISCRETE			
Date: Friday, May 23, 2008	Sheet 27	of			







<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, HsinTaiWu Rd., Hsinchu
Taipai-Hsien221, Taiwan, R.O.C.

Title

KBC_SMSC 1070

Size

A3

Document Number

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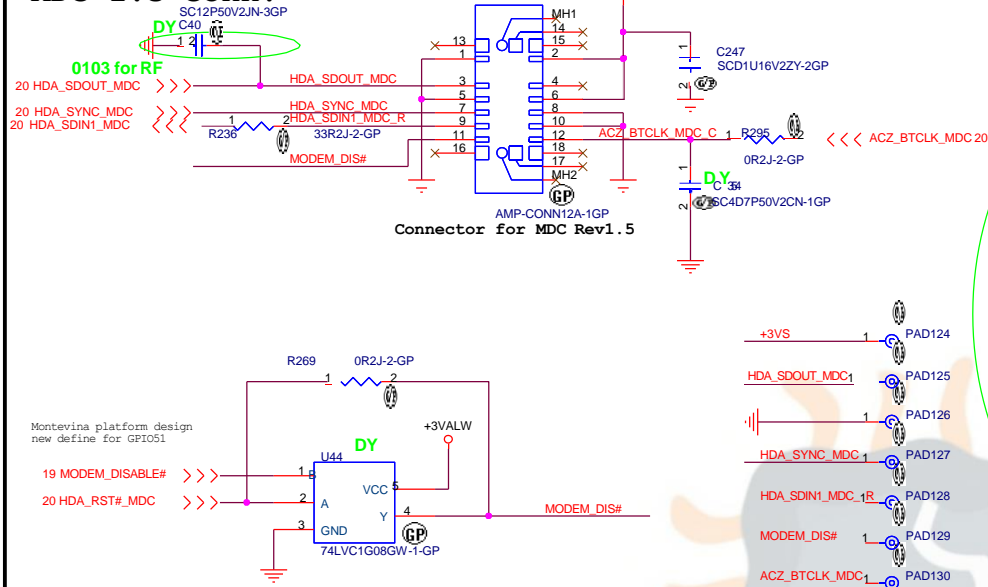
Date: Monday, May 19, 2008

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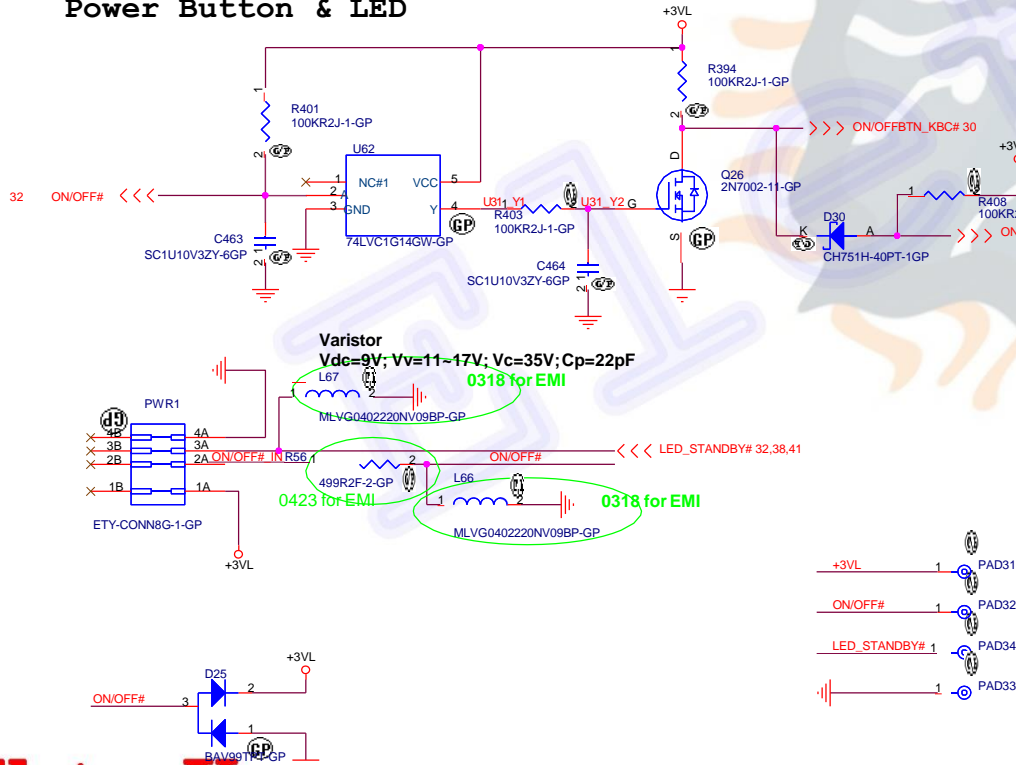
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Eleetro-X

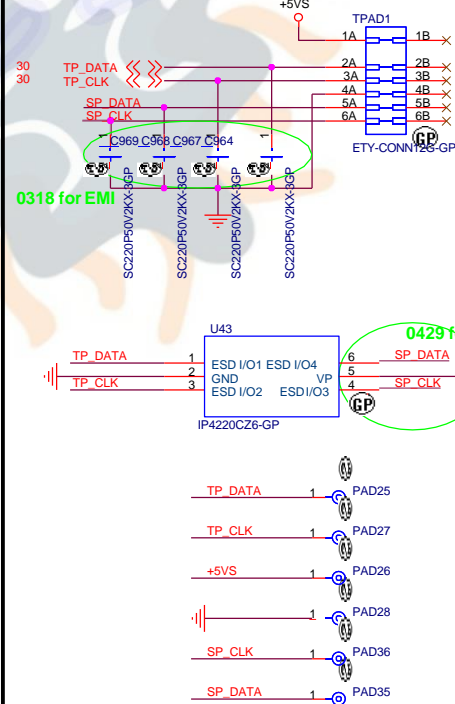
MDC 1.5 Conn.



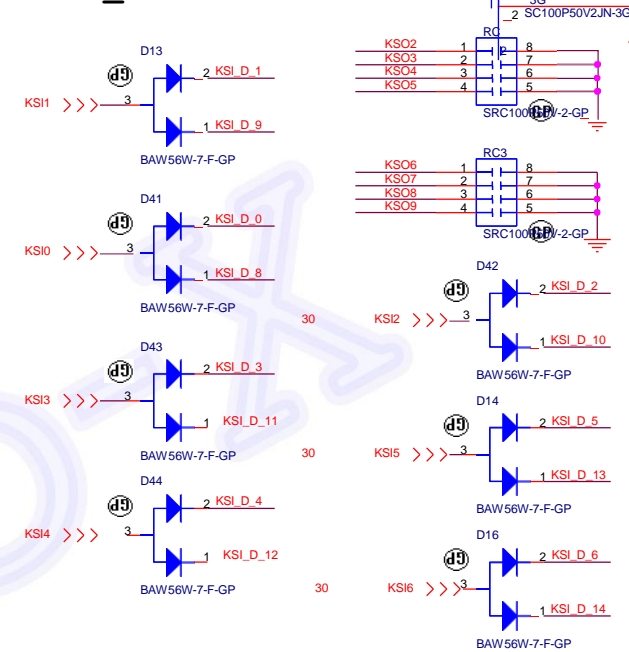
Power Button & LED



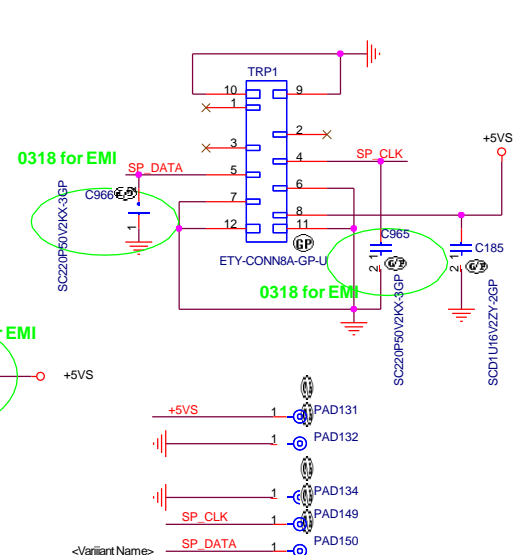
T/P CONN



INT_KBD CONN.



TrackPoint



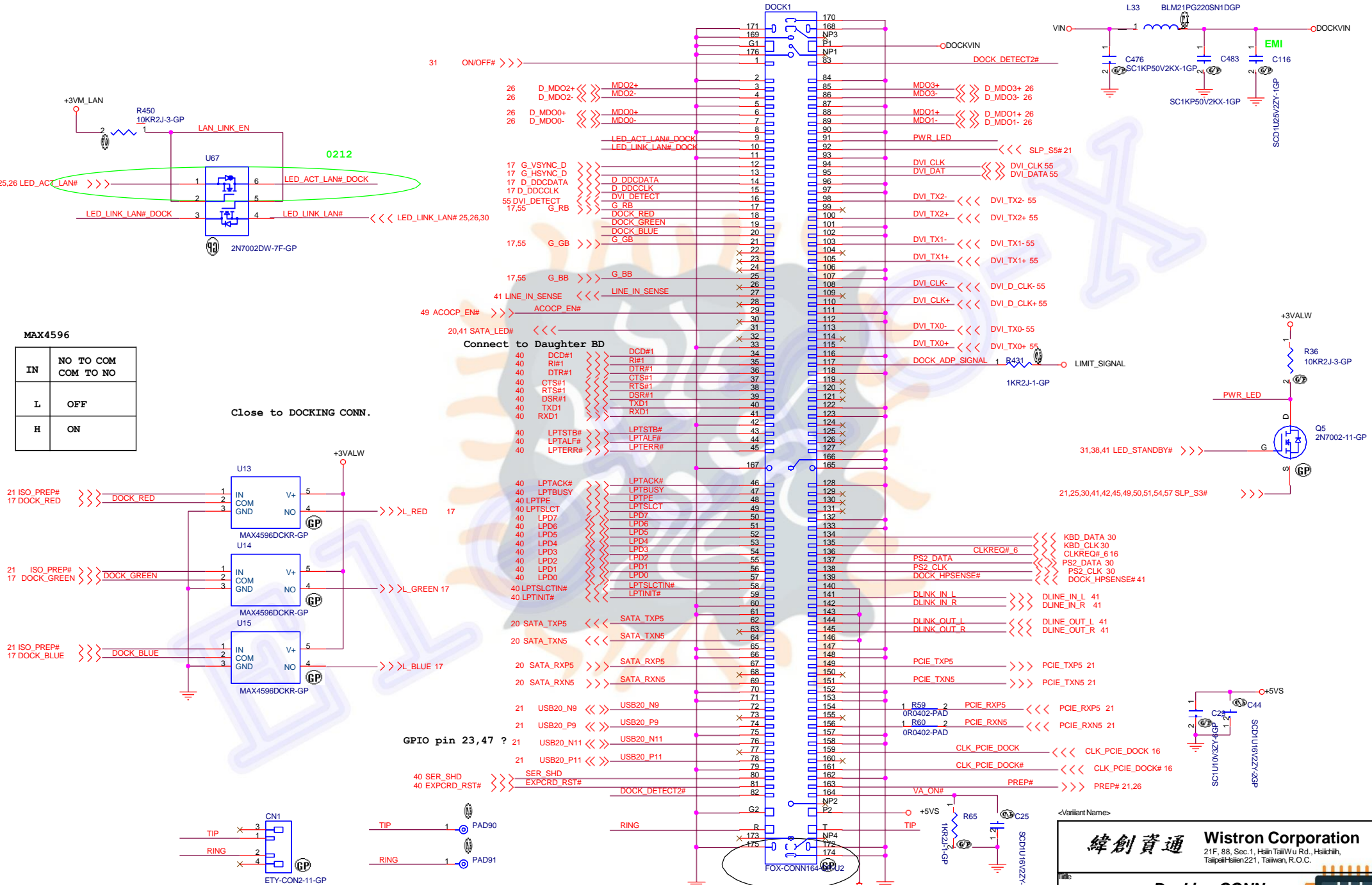
緯創資通 Wistron Corporation
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Taichung-Hsien 221, Taiwan, R.O.C.

MDC/KBD/ON OFF/T.P.
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Docking CONN. 164 PIN

current rating 6A



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Docking CONN

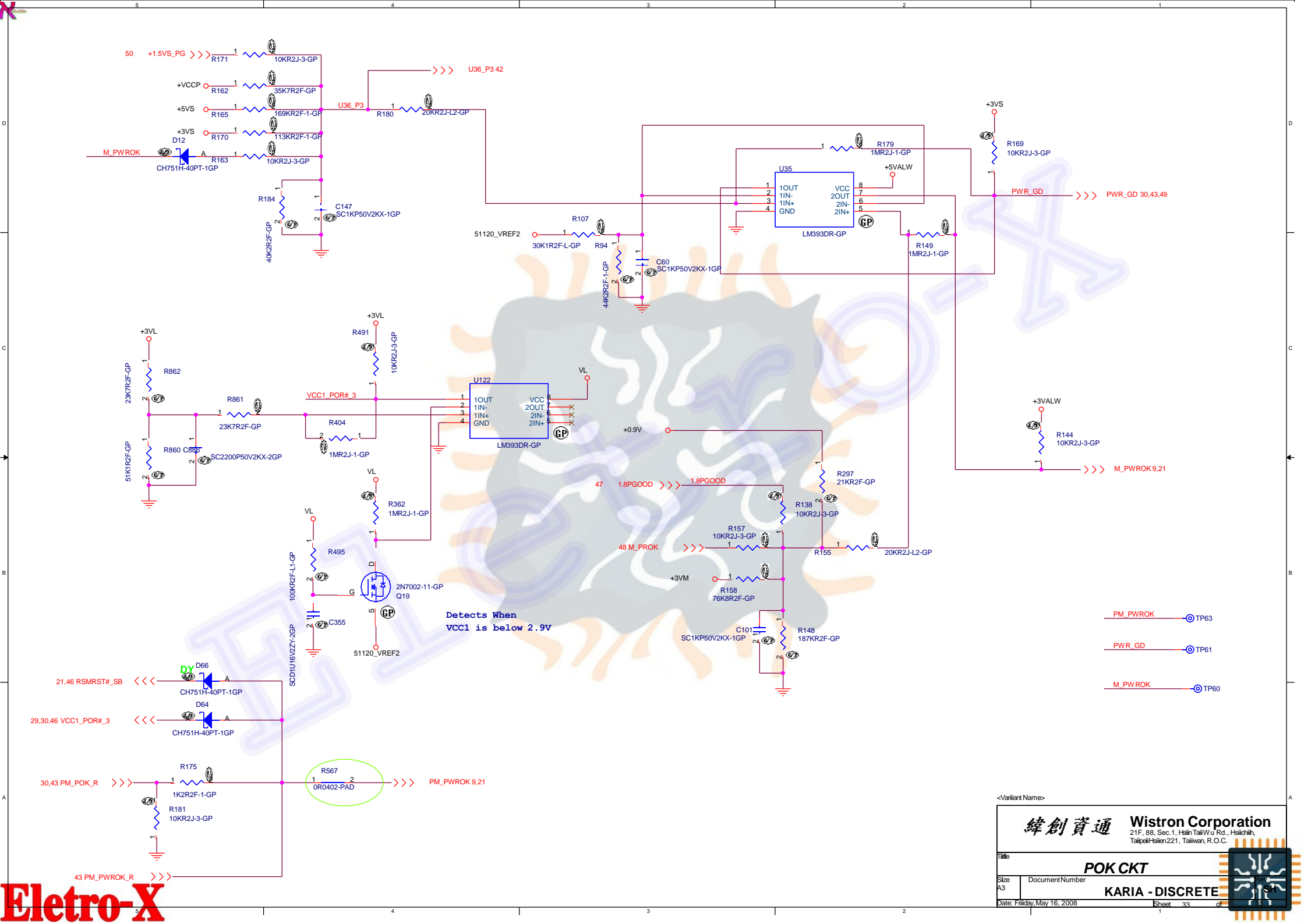
Size A3

Document Number

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KARIA - DISCRETE



Detects When
VCC1 is below 2.9V

- PM_PWROK TP63
- PWR_GD TP61
- M_PWROK TP60

<Variant Name>

緯創資通 Wistron Corporation
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Taipei-Hsien 221, Taiwan, R.O.C.

Title: **POK CKT**

Size: A3 Document Number: **KARIA - DISCRETE**

Date: Friday, May 16, 2008 Sheet: 33 of 33



0423



Current Rating 6 A



CAPS name EMI It Reserve for EMI

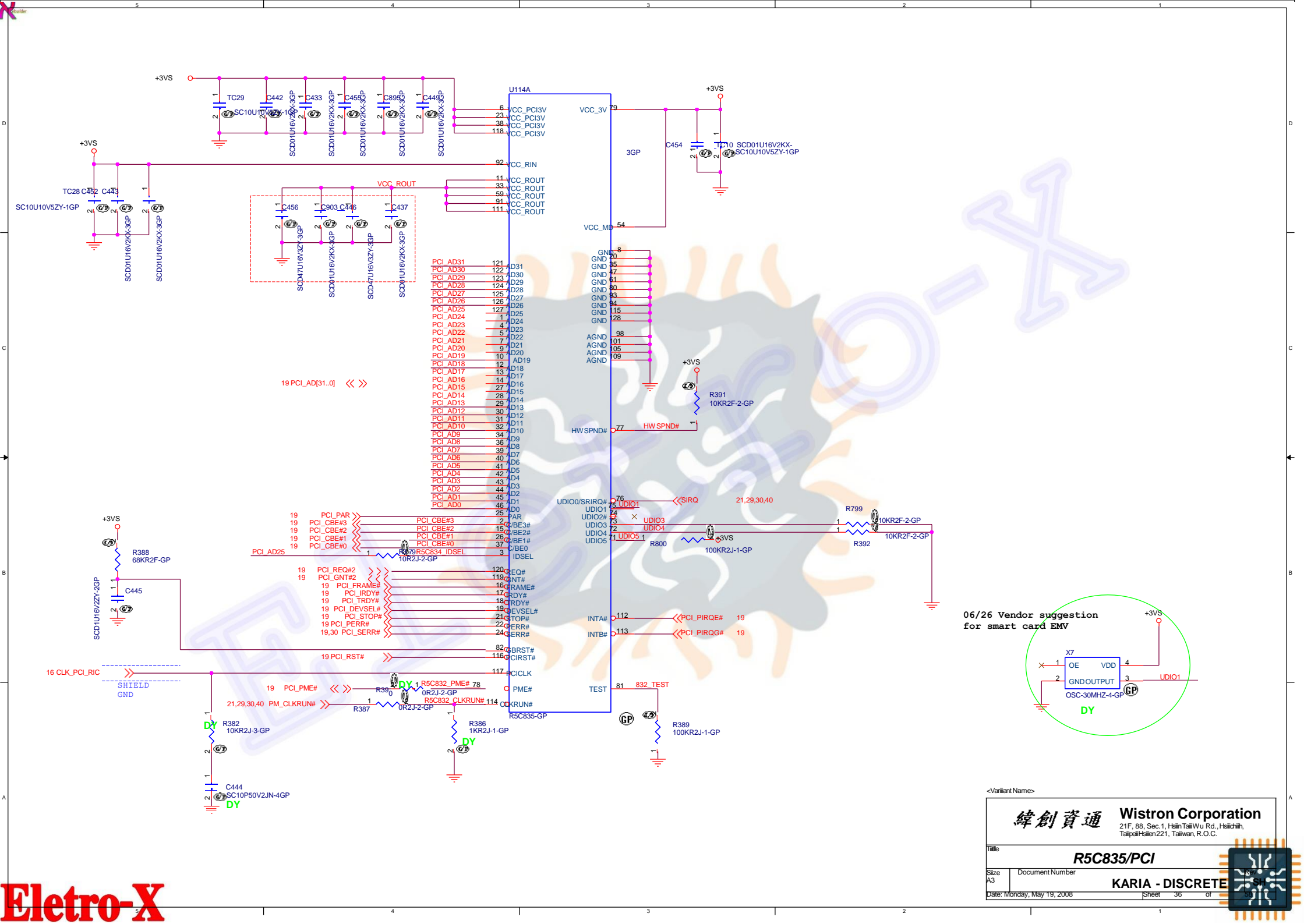


Current Rating 6 A



BATT_B 1 PAD120

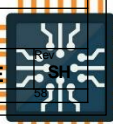


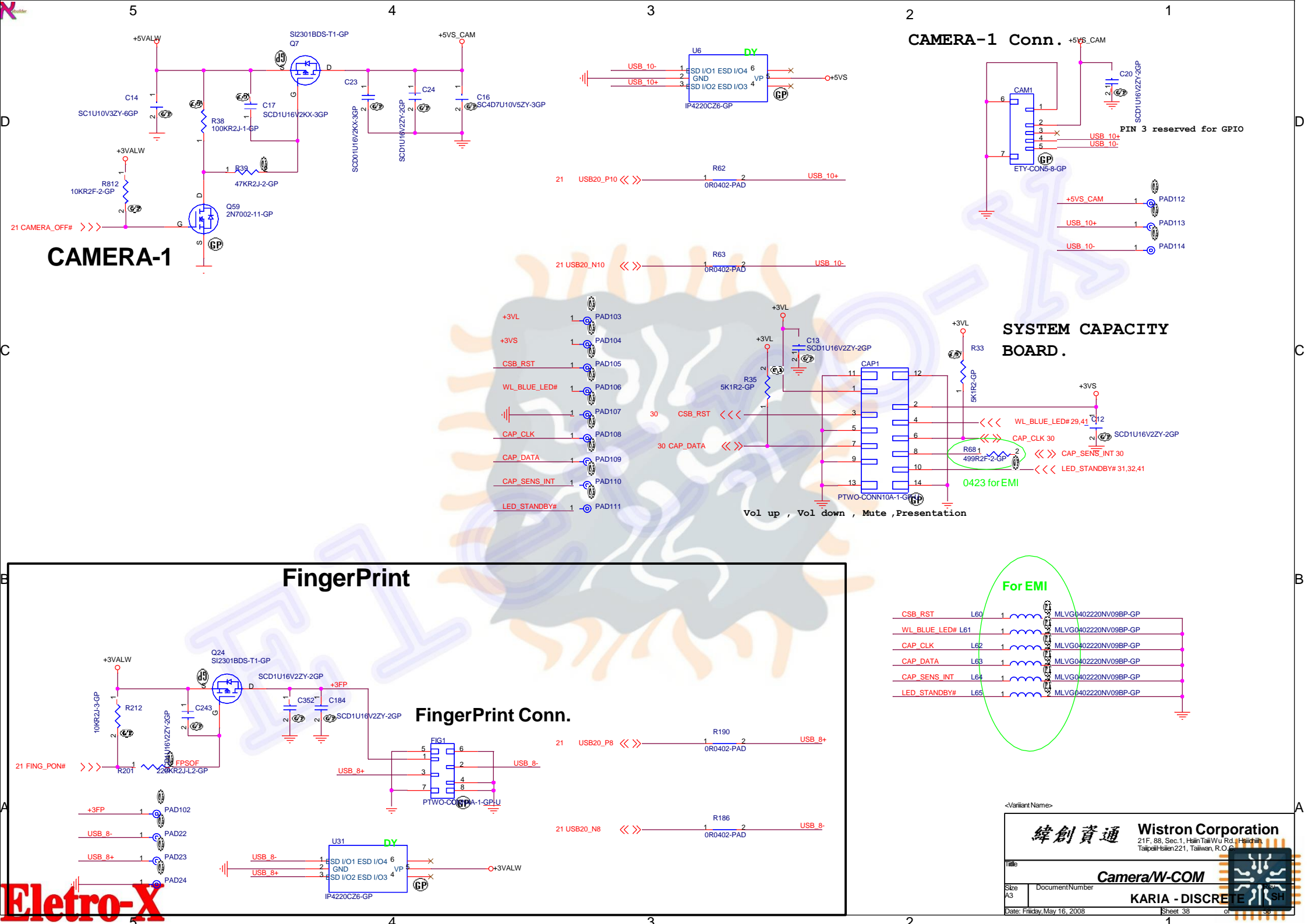


<Variant Name>

緯創資通 Wistron Corporation
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Taippei-Hsien 221, Taiwan, R.O.C.

Title: **R5C835/PCI**
Size: A3 Document Number: **KARIA - DISCRETE**
Date: Monday, May 19, 2008 Sheet: 36 of 36

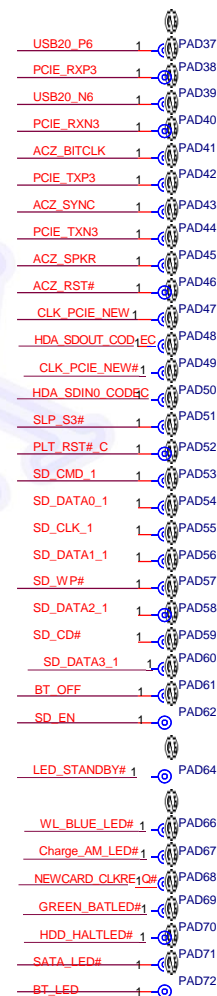
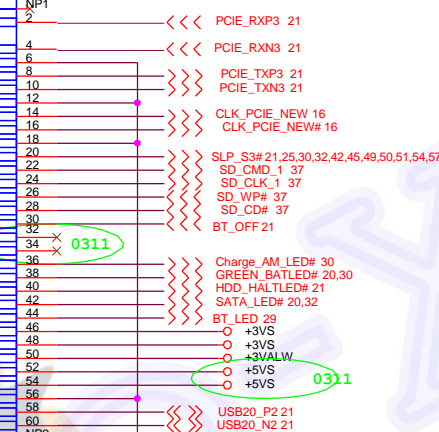
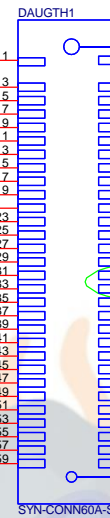
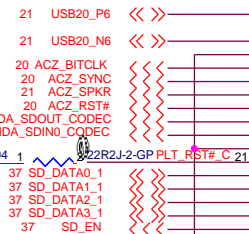
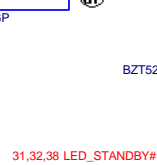
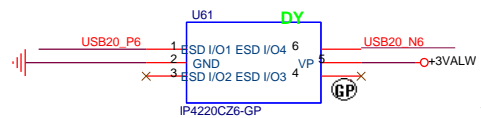




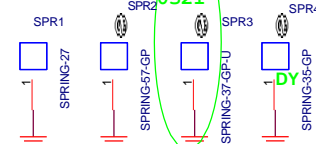
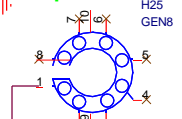
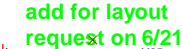
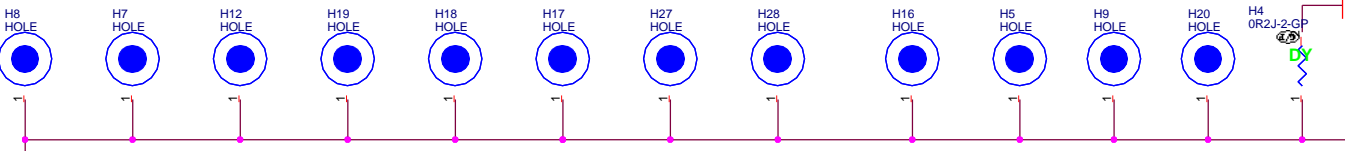
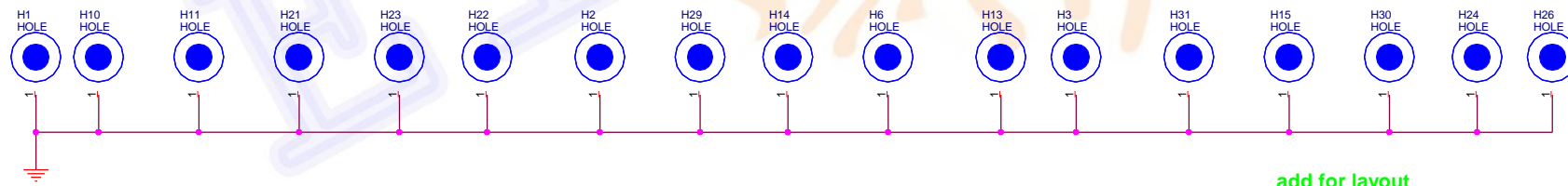
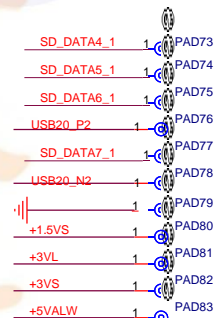
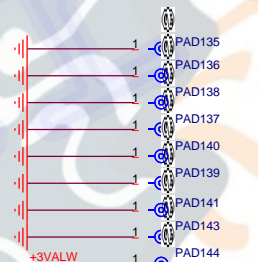
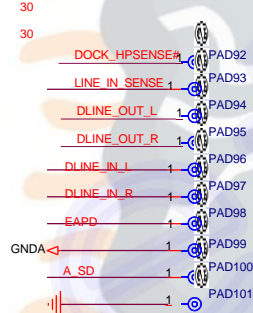
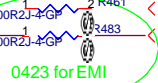
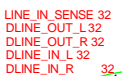
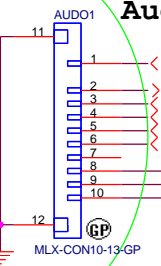
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Daughter Board Connector



Audio Connector



H10,H5 P/N: 34.4V908.001
H27,H28 P/N: 34.4V909.001
H9,H13 P/N:34.4V907.001
H21 P/N:34.4V910.001

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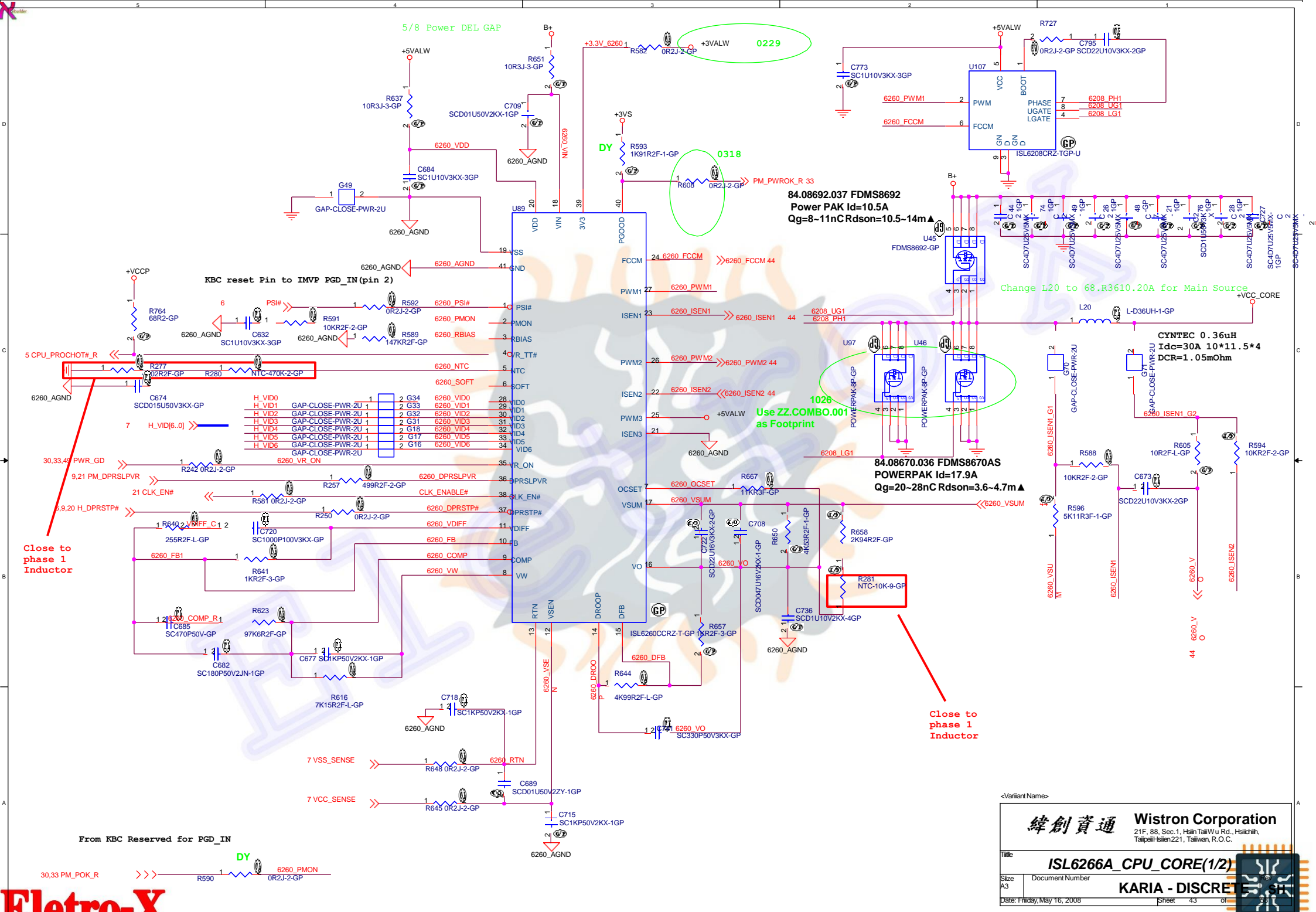
緯創資通	Wistron Corporation 21F, 88, Sec.1, HsinTaiWu Rd., Hsichaih, Taibei-Hsien 221, Taiwan, R.O.C.
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Title: **AUDO/Daughter Connector**

Size: A3 Document Number: **KARIA - DISCRETE**

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Eleto-X



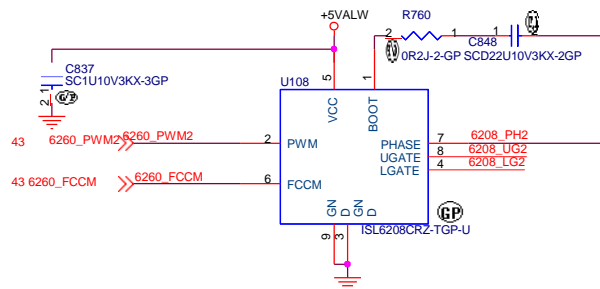
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緯創資通 Wistron Corporation
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Taippei Hsien 221, Taiwan, R.O.C.

Title: **ISL6266A_CPU_CORE(1/2)**

Size: A3 Document Number: **KARIA - DISCRETE**

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84.08692.037 FDMS8692
Power PAK Id=10.5A Qg=8~11nC
Rdson=10.5~14m Δ

1026
Use ZZ.COMBO.001
as Footprint

84.08670.036 FDMS8670AS
POWERPAK Id=17.9A
Qg=20~28nC Rdson=3.6~4.7m Δ

Change L21 to 68.R3610.20A for Main Source

CYNTEC 0.36uH
Idc=30A 10*11.5*4
DCR=1.05mOhm

Panasonic 330uF 2V
ESR=9mfi
Ripple=3A

<Variant Name>

緯創資通 Wistron Corporation
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Taippei Hsien 221, Taiwan, R.O.C.

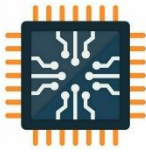
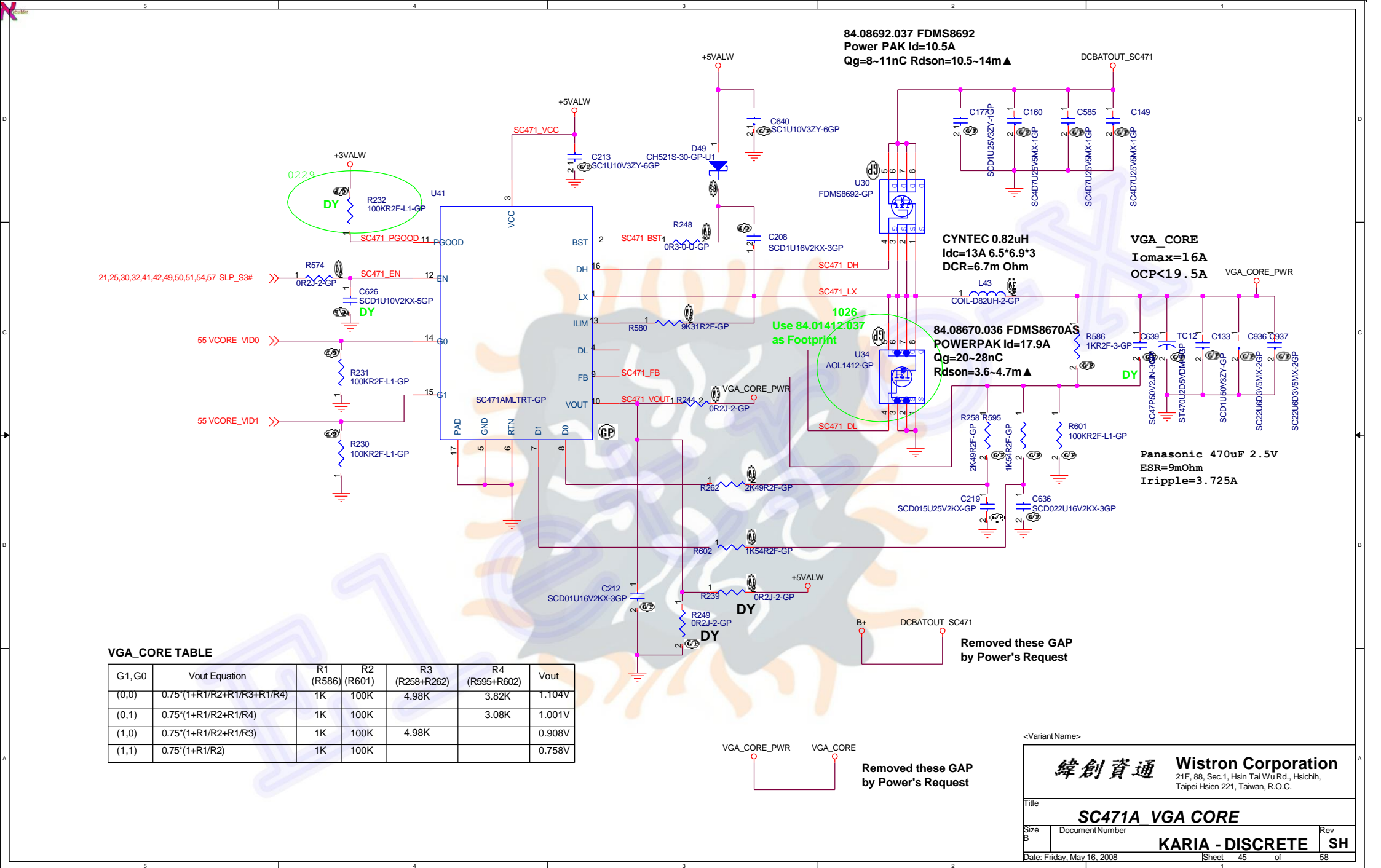
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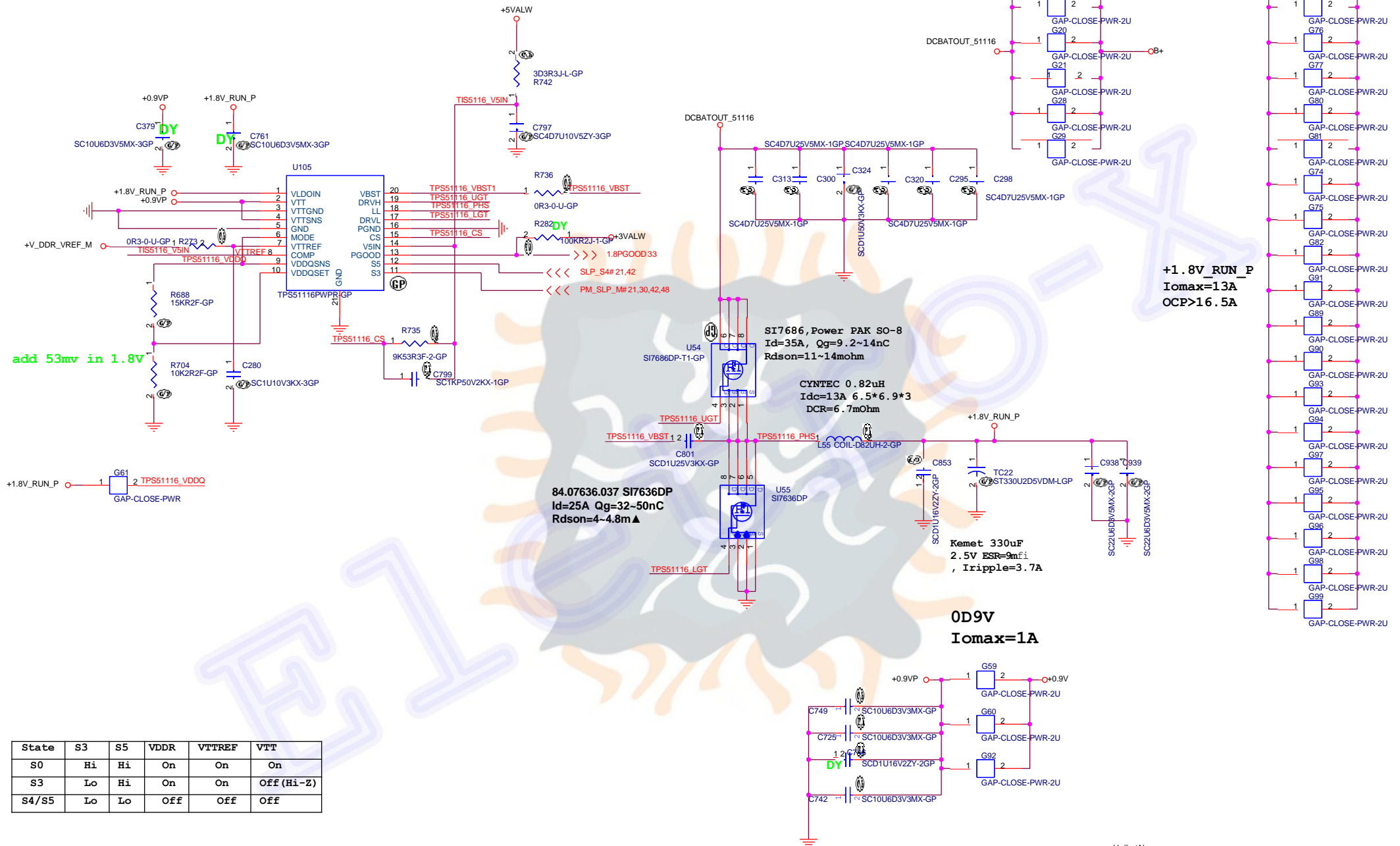
KARIA - DISCRETE

Date: Monday, May 19, 2008

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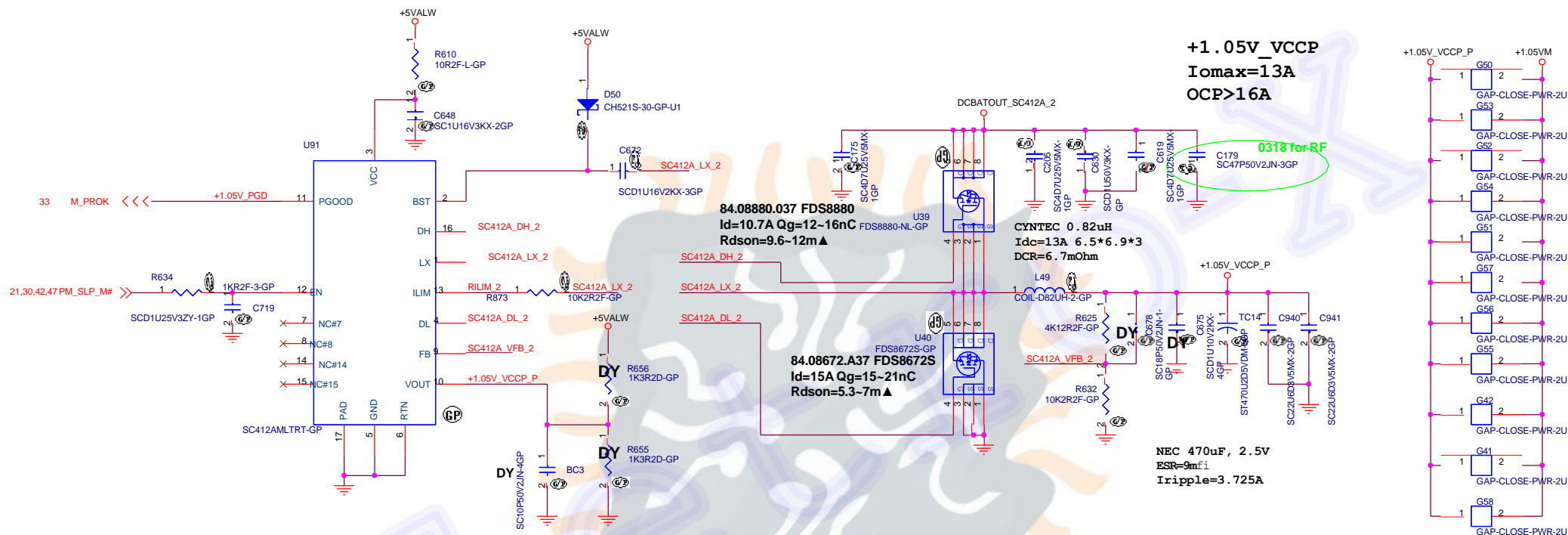


TI TPS51116 for 1D8V and 0D9V



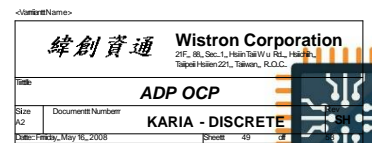
State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

B+ DCBATOUT_SC412A_2

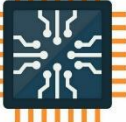


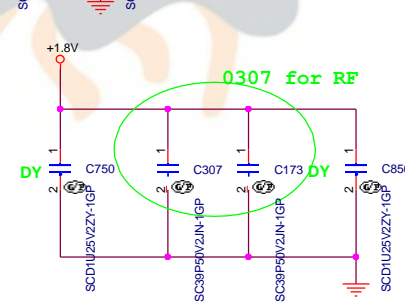
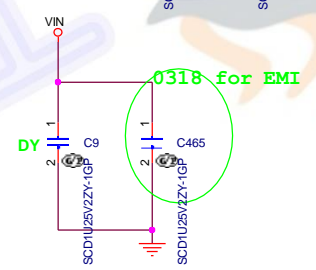
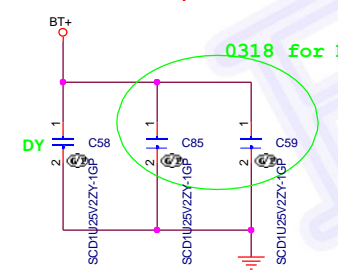
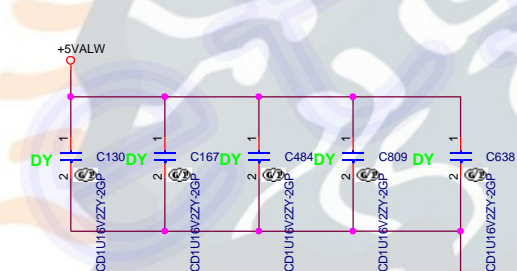
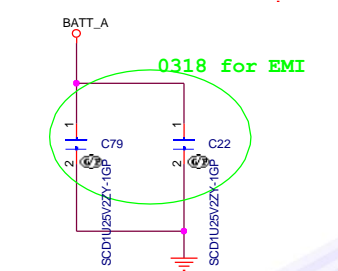
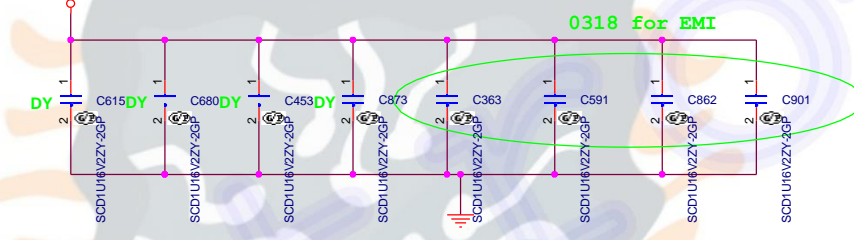
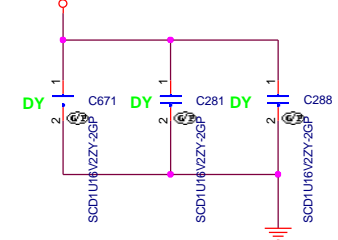
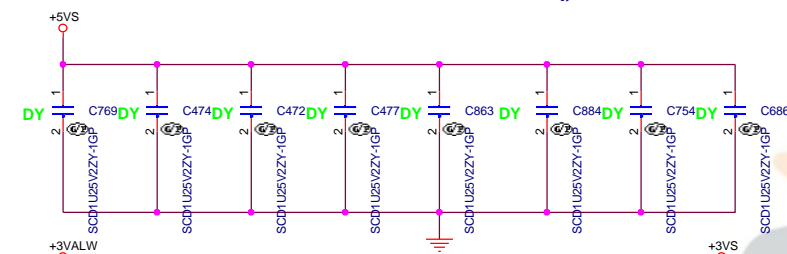
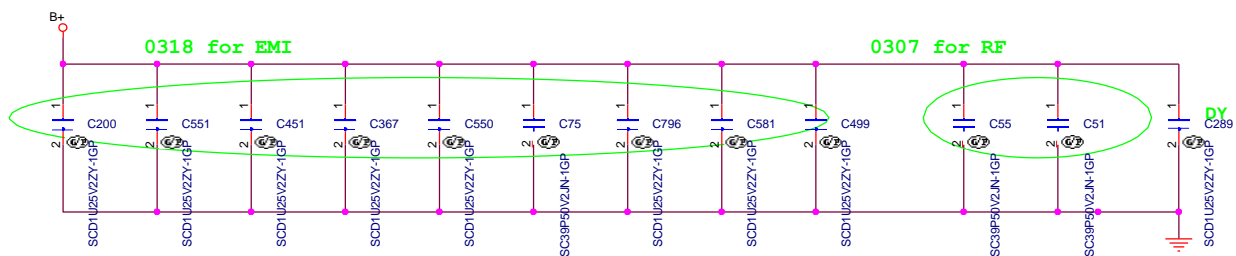
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<Variant Name>

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		21F, 88, Sec.1, Hsin TaiWu Rd., Hsichih, Taipei-Hsien 221, Taiwan, R.O.C.	
File:	EMI CAPS		
Size:	Document Number		
A3			
Date:	Friday, May 16, 2008	Sheet:	52 of 52



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

0 = DON'T INSTALL RES
1 = INSTALL 10K RES
NA = NOT APPLICABLE

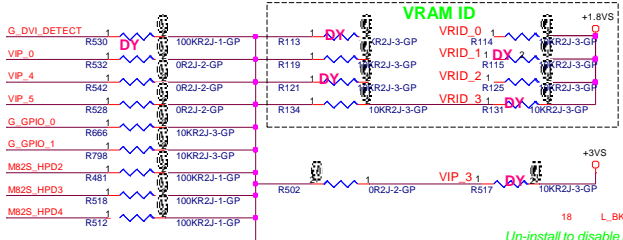
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M82-SCE
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO (M8)	1
BIF_GEN2_EN_A	GPIO5	ALLOW EITHER PCIE 2.5GT/s OR 5GT/s OPERATION	1
ROM_ID_CFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X X
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA
VIP_DEVICE_STRAP_ENA	VSYSN	IGNORE VIP DEVICE STRAPS	0
BIF_VGA_DIS	PSYN	VGA ENABLED	0
BIF_HDMI_EN	HSYN	HDMI ENABLE	1

VRID_[3..0]

00 --> 8M*32
01 --> 16M*32
10 --> 32M*32

00 00
01 01
00 --> Qimonda
01 --> Samsung

VRAM Configuration	Install Resistors	
Samsung 16x32MB	R134, R125, R119, R114	Default
Samsung 32x32MB	R131, R121, R119, R114	
Qimonda 16x32MB	R134, R125, R119, R113	
Qimonda 32x32MB	R131, R121, R119, R113	



Aperture Config	PIN	M82SCE	Strapping Resistor	64MB VRAM	128MB VRAM	256MB VRAM
CONFIG0	GPIO_11	R597	0	0	1	
CONFIG1	GPIO_12	R831	1	0	0	
CONFIG2	GPIO_13	R832	0	0	0	
CONFIG3	GPIO_9	TP88	X	X	X	

